

# Compal Confidential

ELMV2

DIS M/B Schematics Document

Intel Kabylake RU Processor with DDR4

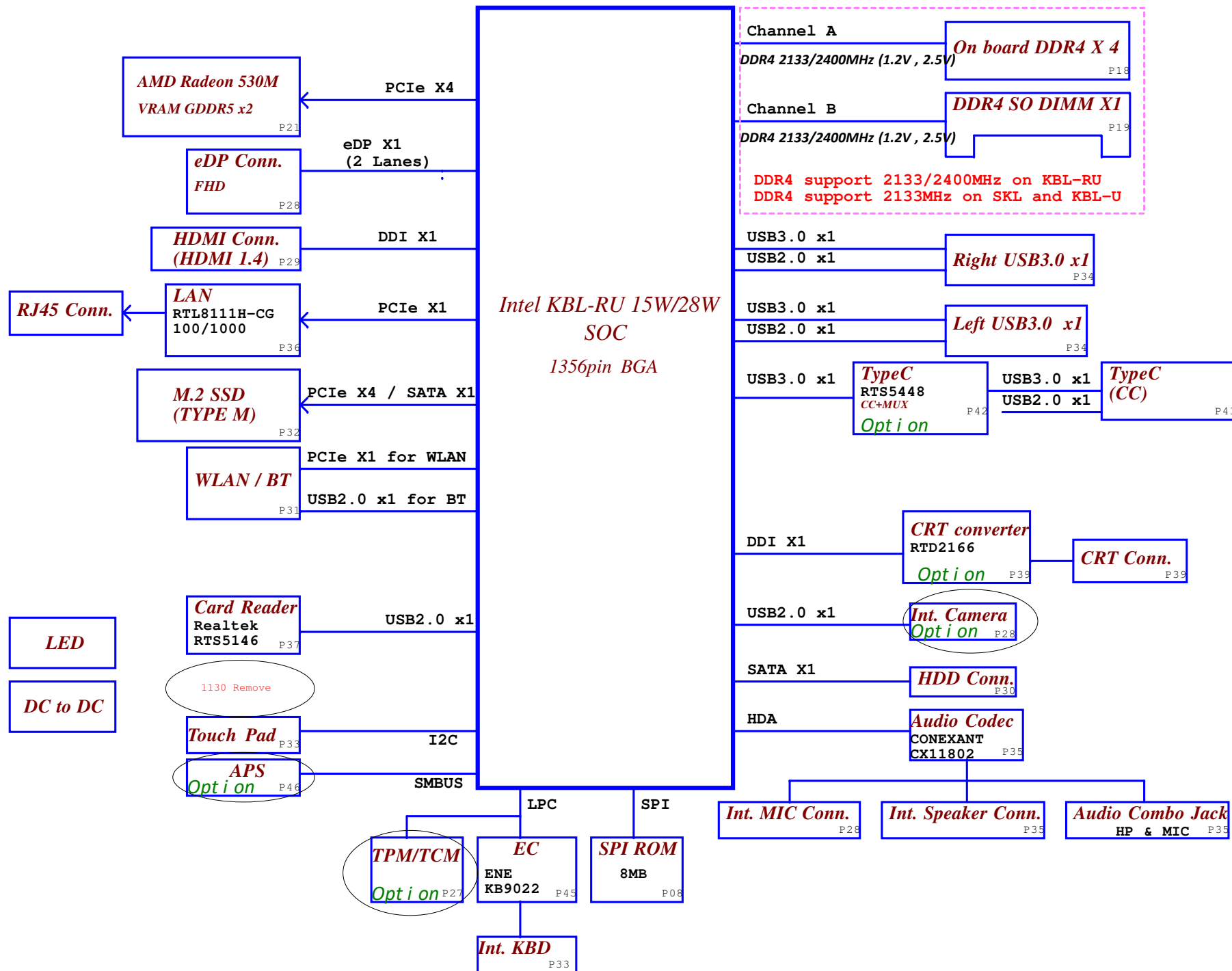
AMD R17M

2017-11-06

LA-F486P

REV : 0 . 1

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## Voltage Rails

power plane	+RTCBATT	+B +5VL +3VL	+5VALW +3VALW +1.8VALW +1VALW	+1.0V_VCCST +2.5V +1.2V	+5VS +3VS +3VGS +1.8VGS +1.0VS_VCCIO +PCIE_VGS +VGA_CORE +1.35VS_VRAM +0.6VS +VCCCORE +VCCGT +VCCSA
State					
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 and S4/AC	O	O	O	X	X
S5 and S4/Battery only	O	O	X	X	X
S5 and S4/AC&Battery don't exist(Only RTC )	O	X	X	X	X

## EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

## PCH SM Bus address

Device	Address
DDR_JDIMM1	1010 000x A0h
RTD2166	1100 100 A0h

## SMBUS Control Table

	SOURCE	GPU	BATT	NECP388	SODIMM	SOC
SMB_EC_CK1	EC KB9022	X	V	X	X	X
SMB_EC_DA1	+3VALW		+3VALW			
SMB_EC_CK2	EC KB9022	V	X	X	X	V
SMB_EC_DA2	+3VS	+3VGS				+3VALW
PCH_SMBCLK	PCH	X	X	X	V	X
PCH_SMBDATA	+3VALW				+3VS	
PCH_SML0CLK	PCH	X	X	X	X	X
PCH_SML0DATA	+3VALW					
SML1CLK	PCH	V	X	V	X	X
SML1DATA	+3VALW	+3VGS		+3VS		

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V (RAM)	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## USB 2.0 Port Table

Port	3 External USB Port
1	USB 3.0 Port
2	USB 3.0 Port
3	TYPE-C USB 3.0 Port
4	
5	Camera
6	M.2 BT
7	Card Reader
8	
9	
10	

## USB 3.0 Port Table

Port	USB 3.0 Port
1	USB 3.0 Port
2	USB 3.0 Port
3	TYPE-C USB 3.0 Port
4	
5	
6	

## SATA Port Table

Port	
0	HDD
1	
2	M.2 SATA SSD

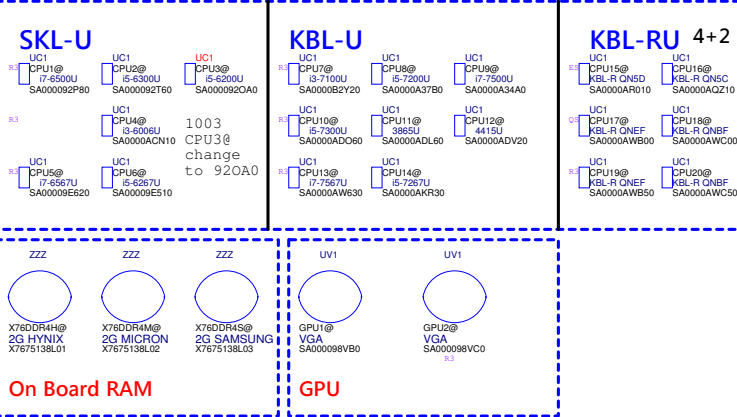
## PCIe Port Table

Port	Lane	
1	1	GPU
2	2	
3	3	
4	4	
5		LAN
6		M.2 WLAN+BT
7		
8		
9		
10		M.2 PCIe*4 SSD
11		
12		

## CPU

2+2

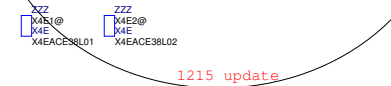
2+3



## BOM Structure Table

Item	BOM Structure
SKL only	SKL@
For 2+2	U22@
For 4+2	U42@
For DIS	DIS@
For UMA	UMA@
EMI pop	EMI@
EMI Un-pop	@EMI@
ESD pop	ESD@
ESD Un-pop	@ESD@
RF pop	RF@
RF unpop	@RF@
For SPI 8M	8M@
NONAOU	NONAOU@
NO 2nd Battery	NOBATT2@
Camera	CMOS@
TPM	TPM@
TCM	TCM@
NO TPM/TCM	NOTPM@
TYPEC 5448	TYPEC@
NONTYPEC	NONTYPEC@
APS	APS@
NOAPS	NOAPS@
CRT@	CRT@
SPEAKER STEREO	STE@
SPEAKER MONO	MONO@
Onboard RAM HYNIX	X76DDRH@
Onboard RAM MICRON	X76DDRM@
Onboard RAM SAMSUNG	X76DDRS@
VRAM HYNIX	X76H2G@
VRAM MICRON	X76M4G@
VRAM SAMSUNG	X76S2G@
Connector	ME@

X4E	TYPEC_5448	CRT
X4EACE38L01	Y	Y
X4EACE38L02	N	Y



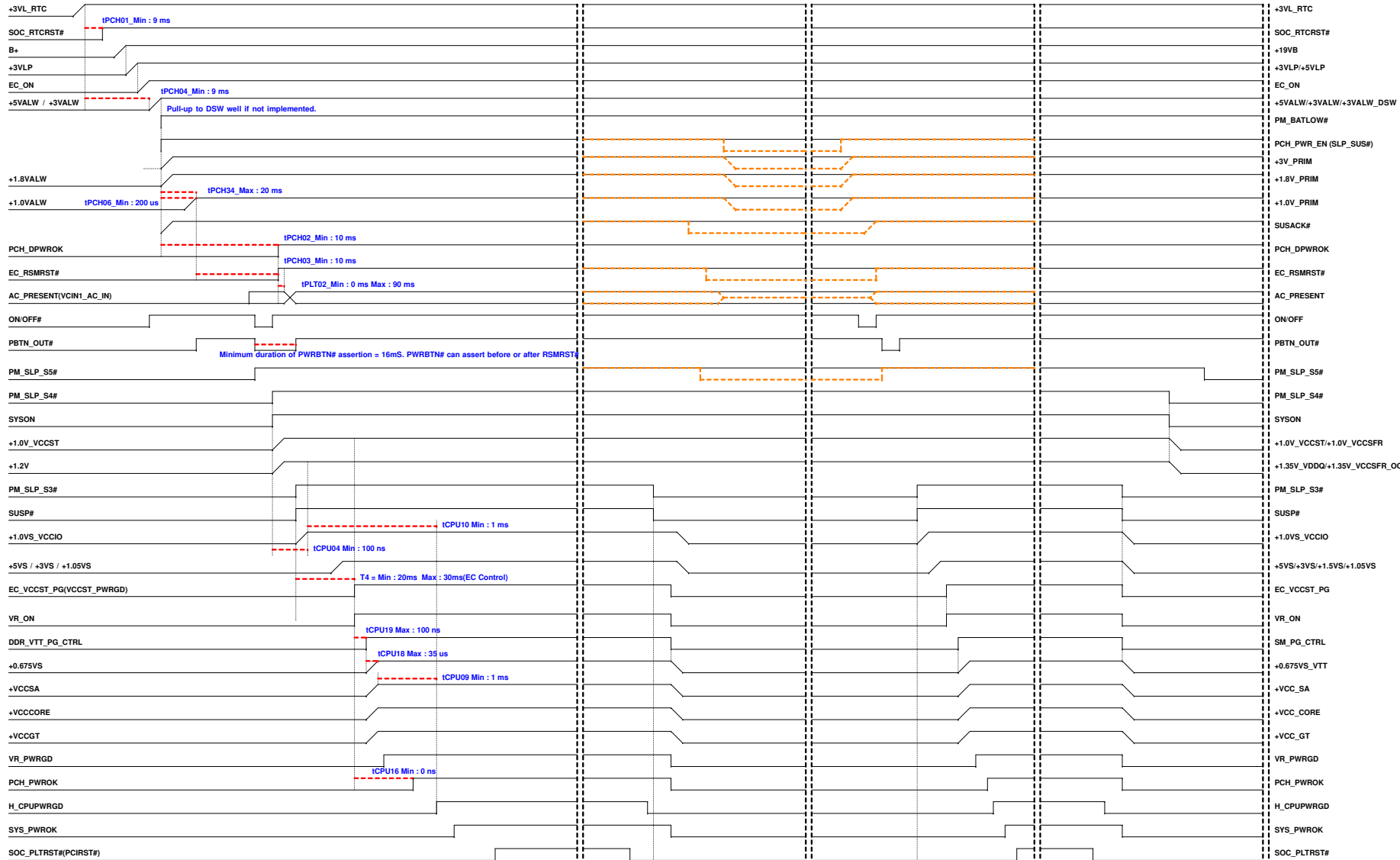
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G3→S0

S0→S3/DS3

S3/DS3→S0

S0→S5



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M1-30 VRAM STRAP

X76@		X76@					
Vendor UV3, UV4, UV5, UV6		ID	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV22	R_pd RV27
X76S2G@ X7675138L06	SAMSUNG 4096Mbits 2GBytes SA000092D30 256M32 R4G80325FB-HC28	0	0	0	0	NC	4.75K
X76H2G@ X7675138L04	HYNIX 4096Mbits 2GBytes SA00009U130 256M32 H5GC8H24MJR-R0C	1	0	0	1	8.45K	2K
X76M2G@ X7675138L05	MICRON 4096Mbits 2GBytes SA00009TV20 256M32 MT51J256M32HF-70:A	2	0	1	0	4.53K	2K
		4	1	0	0	4.53K	4.99K
		5	1	0	1	3.24K	5.62K
		6	1	1	0	3.4K	10K



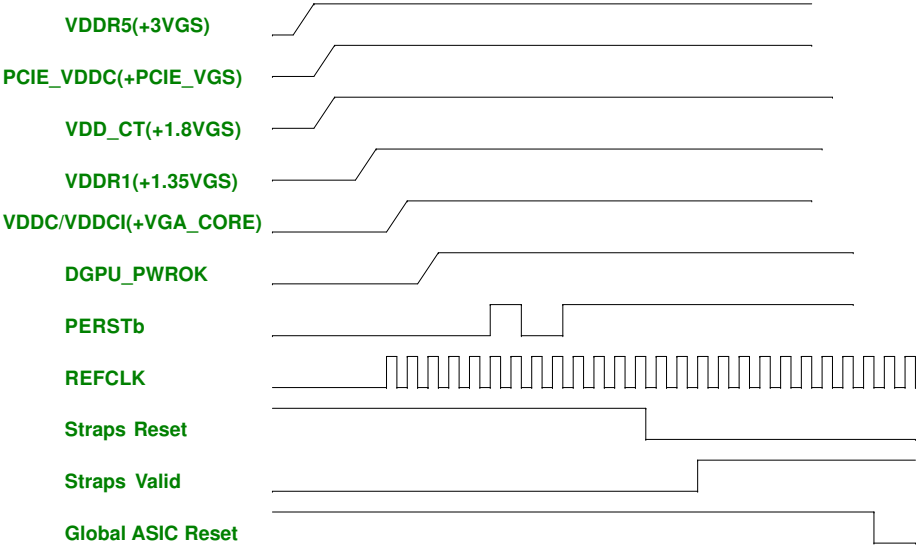
R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Power-Up/Down Sequence

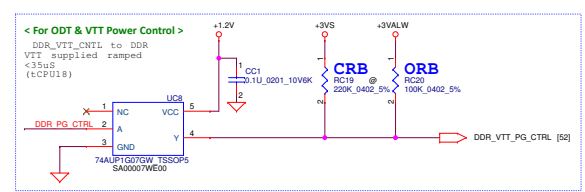
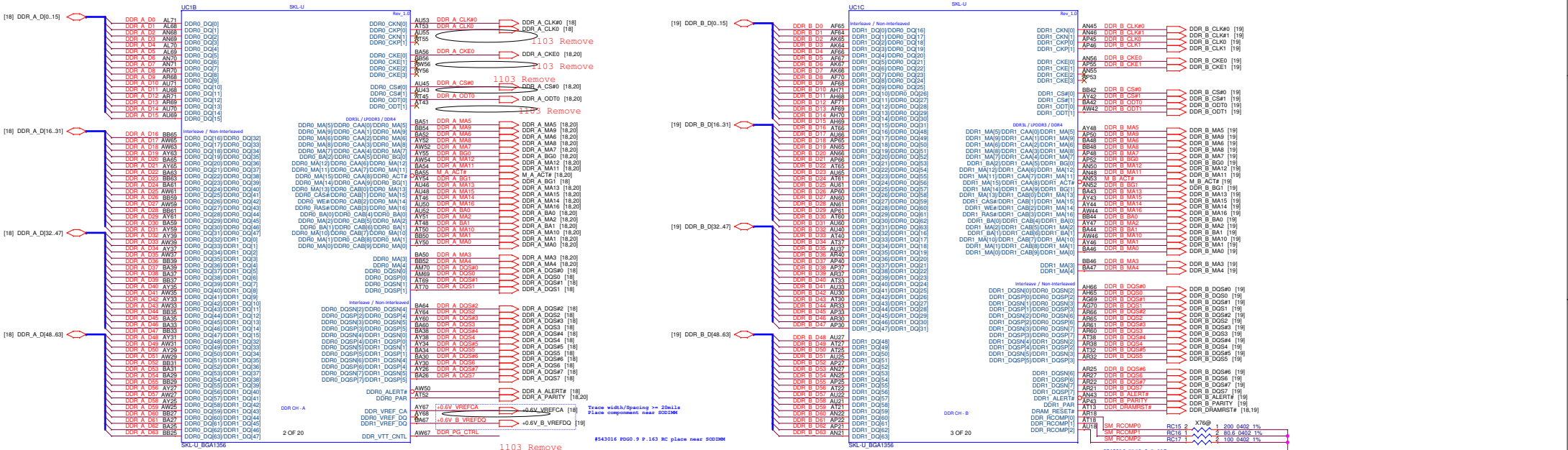
"M1" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- It is recommended that the 3.3-V rail ramp up first.
- It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2ms from the start of VDDC ramping up.
- The power rails that are shared with other components on the system should be gated for the dGPU so that when dGPU is powered down (for example AMD PowerXpress™ idle state), all the power rails are removed from the dGPU.
- The gate circuits must meet the slew rate requirement (such as ≤ 50mV/us)
- VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



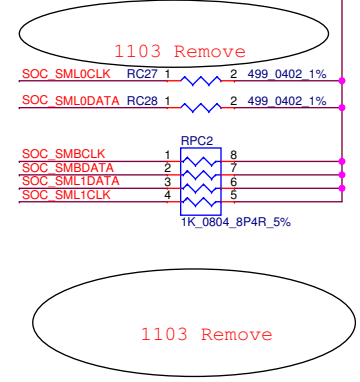
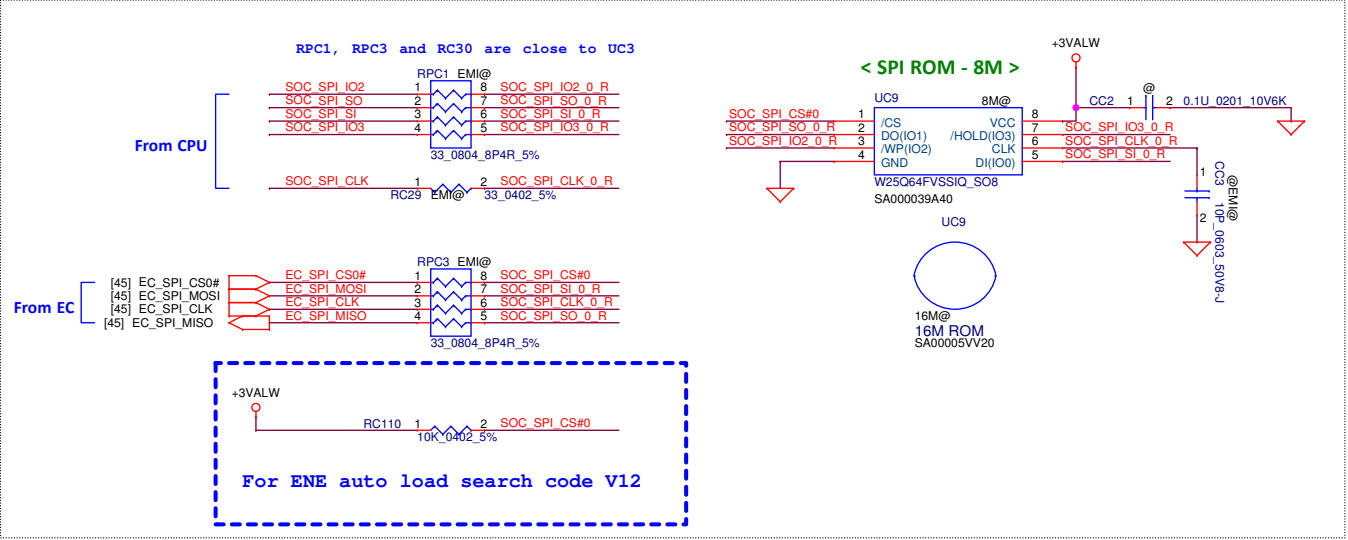
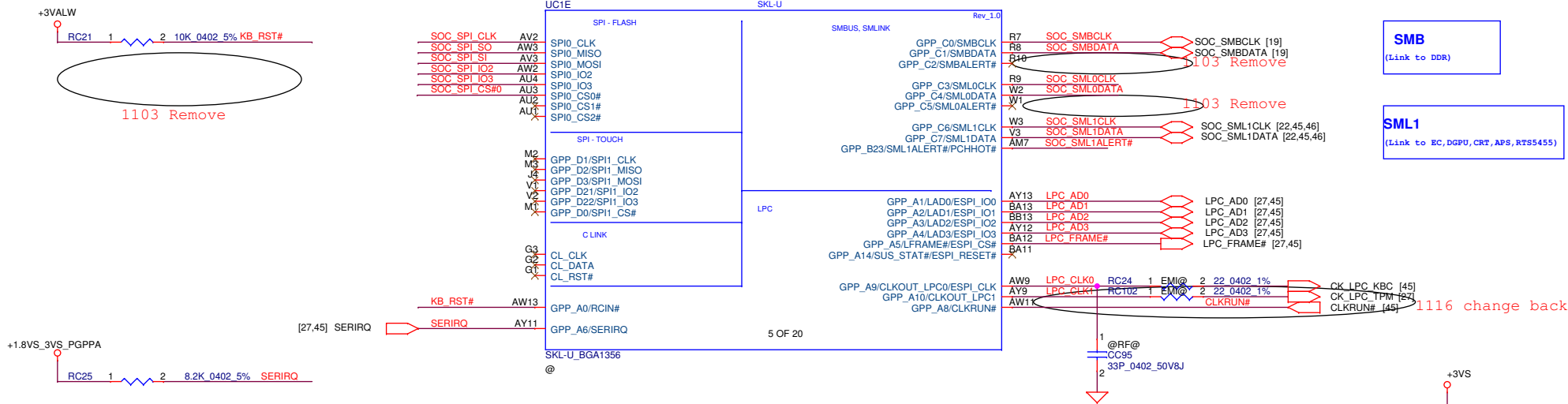


# Interleaved Memory



	SDP	DDP
RC15	200 1%	121 1%

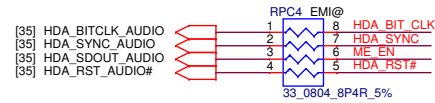
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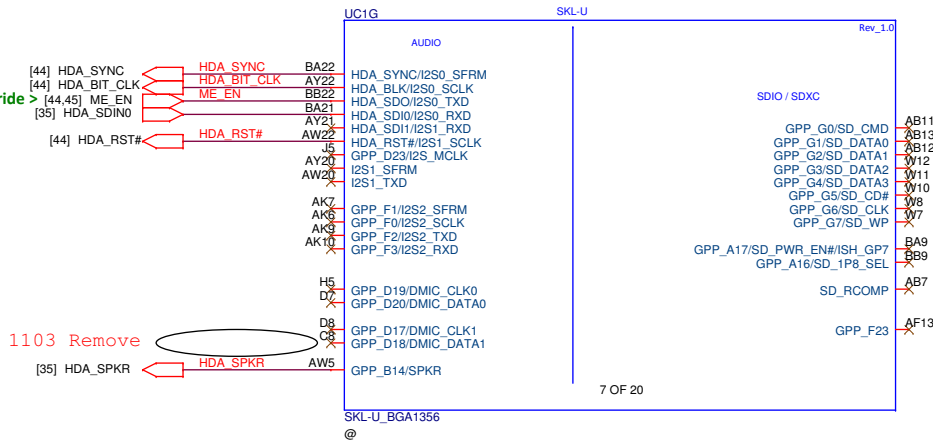
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< HD AUDIO >



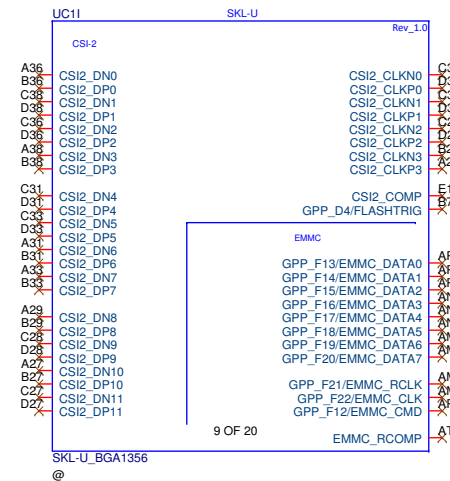
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1103 Remove

1103 Remove

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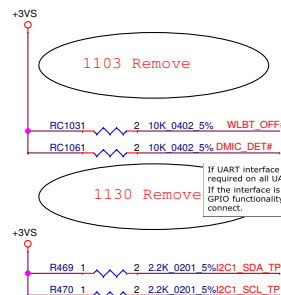
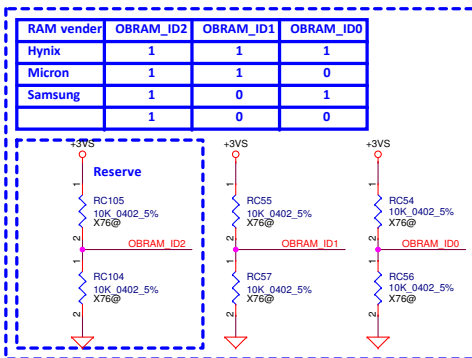


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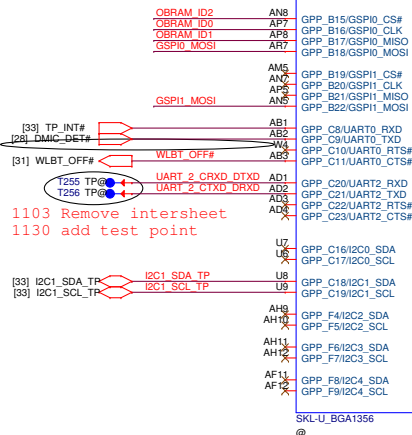
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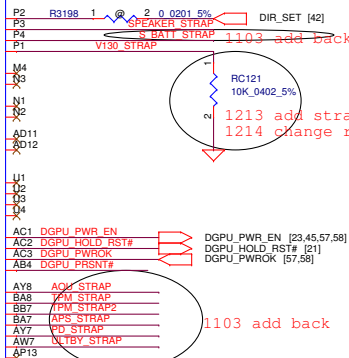
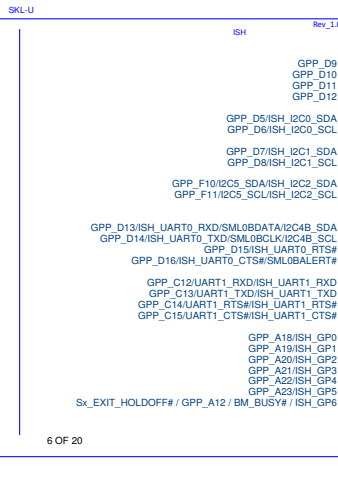




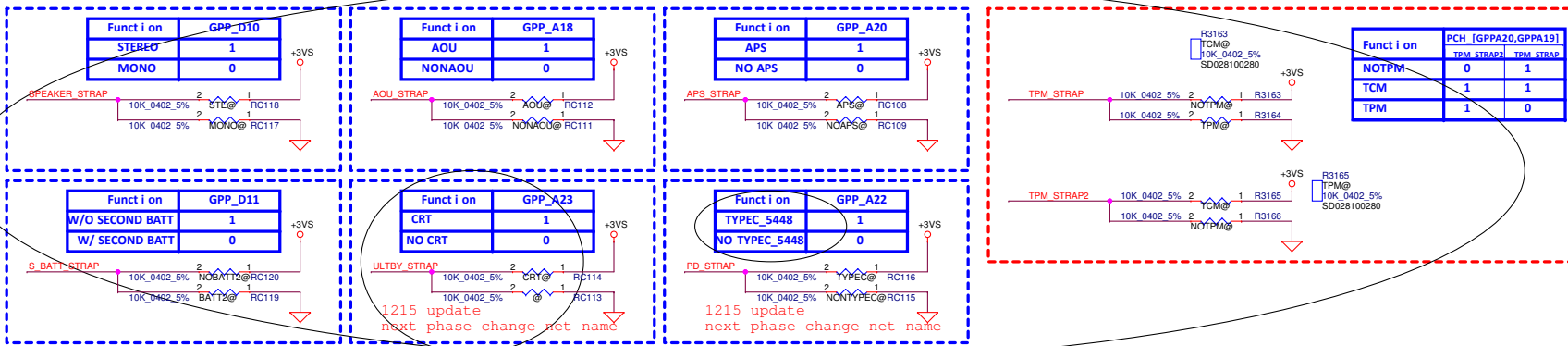
1102 Remove



1103 Remove intersheet  
1130 add test point

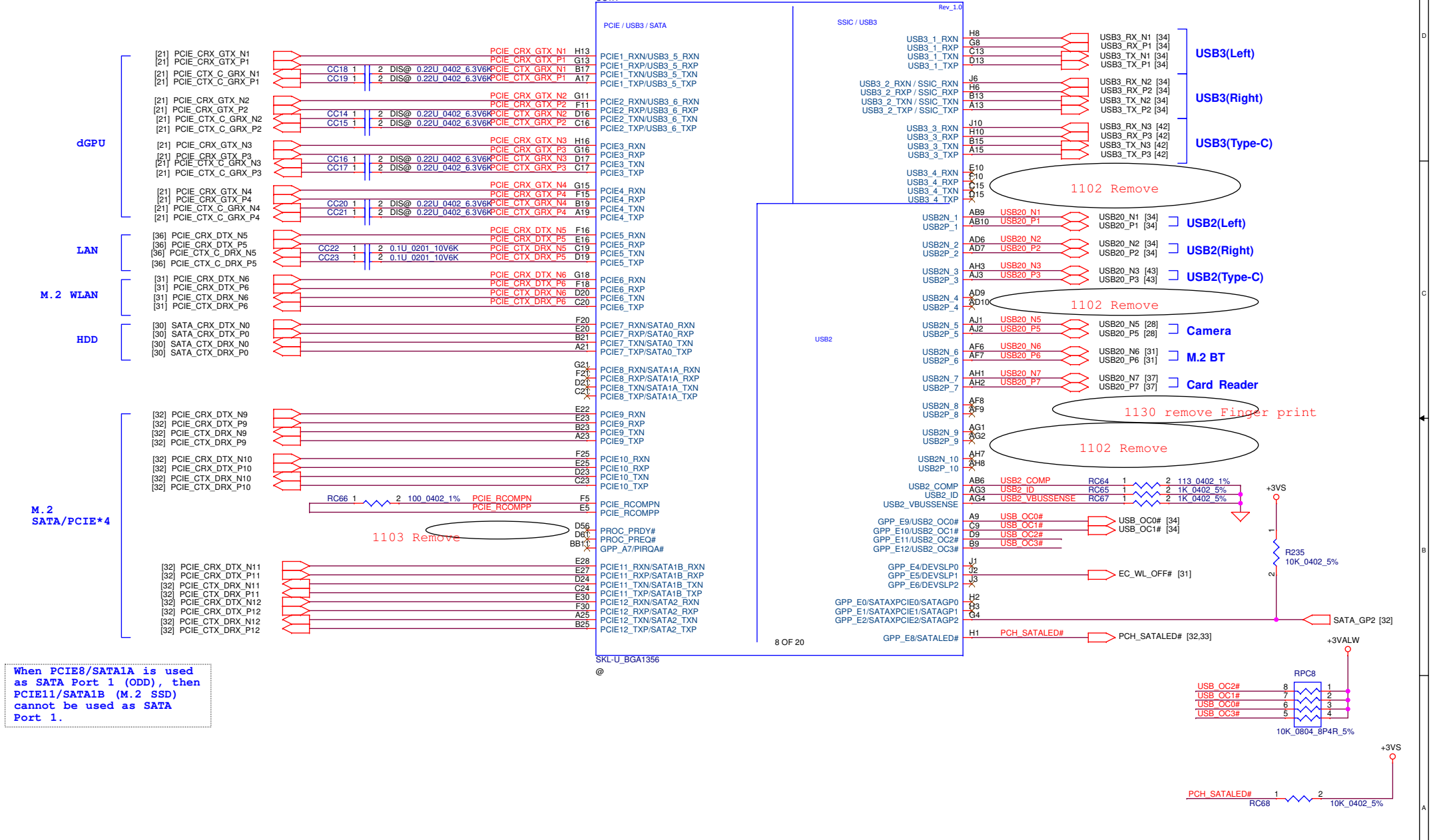


Function	GPP_C15
UMA	1
DIS	0



1103 add back

When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

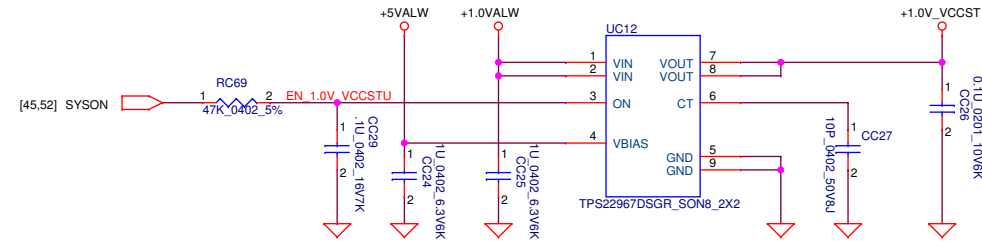


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Follow 543977\_SKL\_PDDG\_Rev0\_91  
CC24 10PF ->22us(Spec:<= 65us)

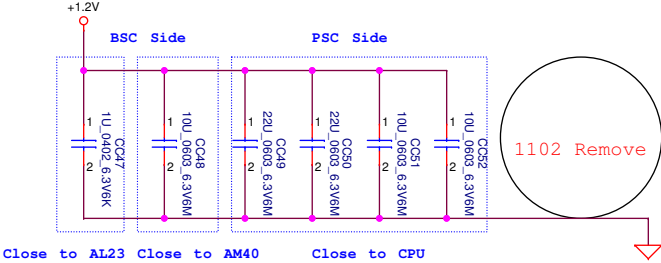
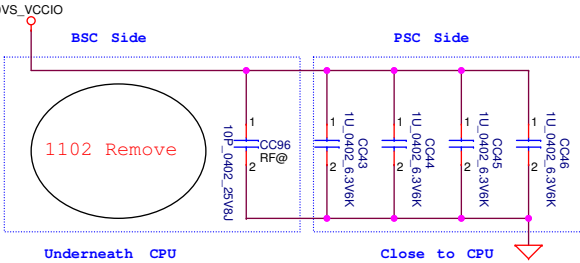
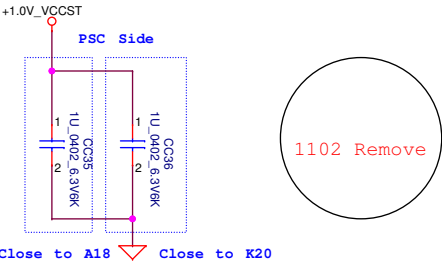
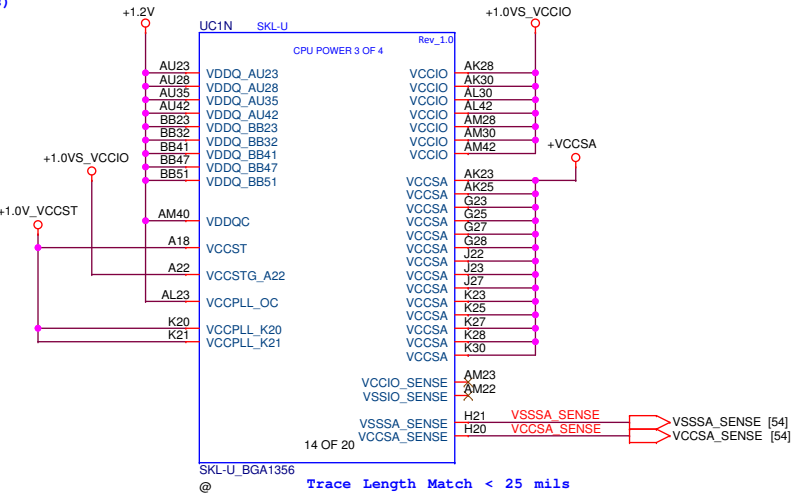
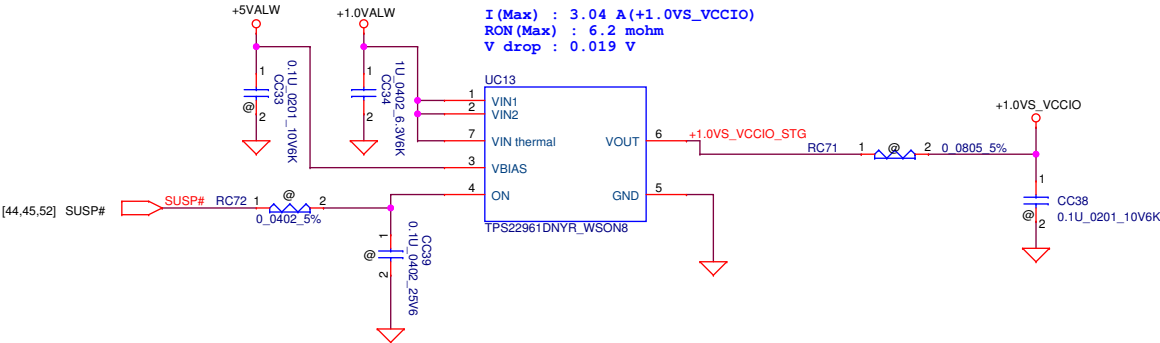
+1.0VALW TO +1.0V\_VCCST

I(Max) : 0.16 A(+1.0V\_VCCST)  
RON(Max) : 25 mohm  
V drop : 0.004 V

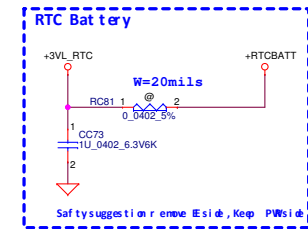
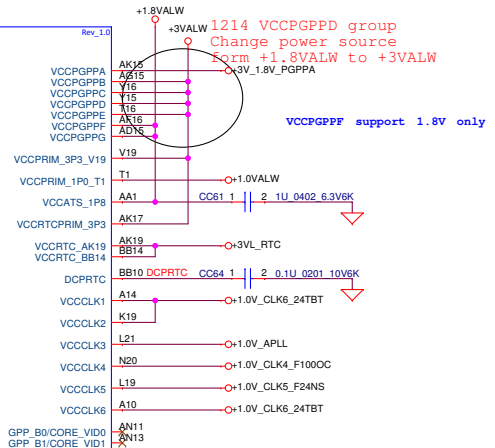
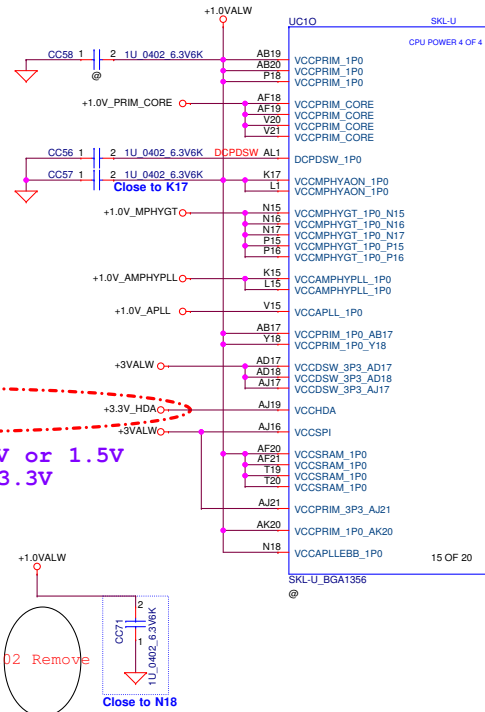
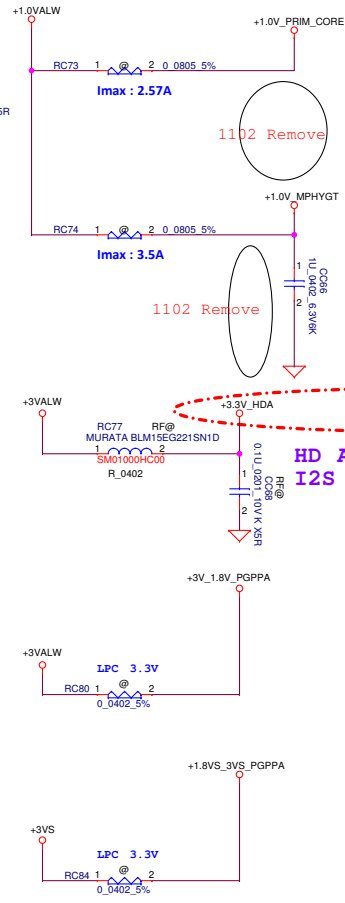
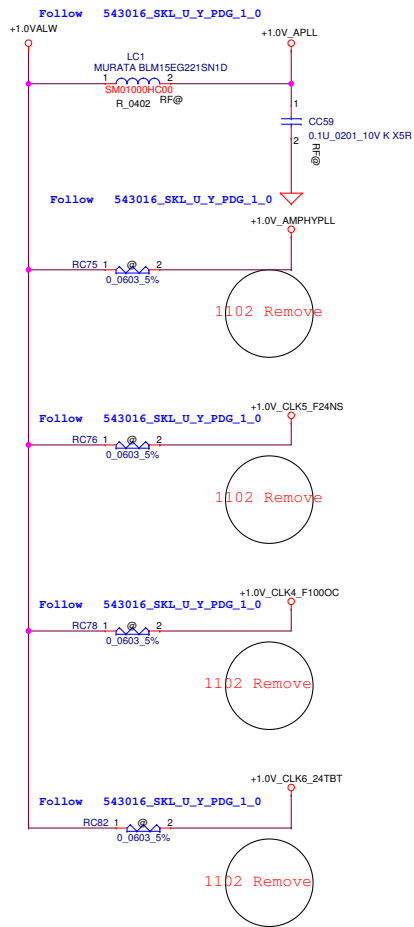


+1.0VALW TO +1.0VS\_VCCIO

I(Max) : 3.04 A(+1.0VS\_VCCIO)  
RON(Max) : 6.2 mohm  
V drop : 0.019 V



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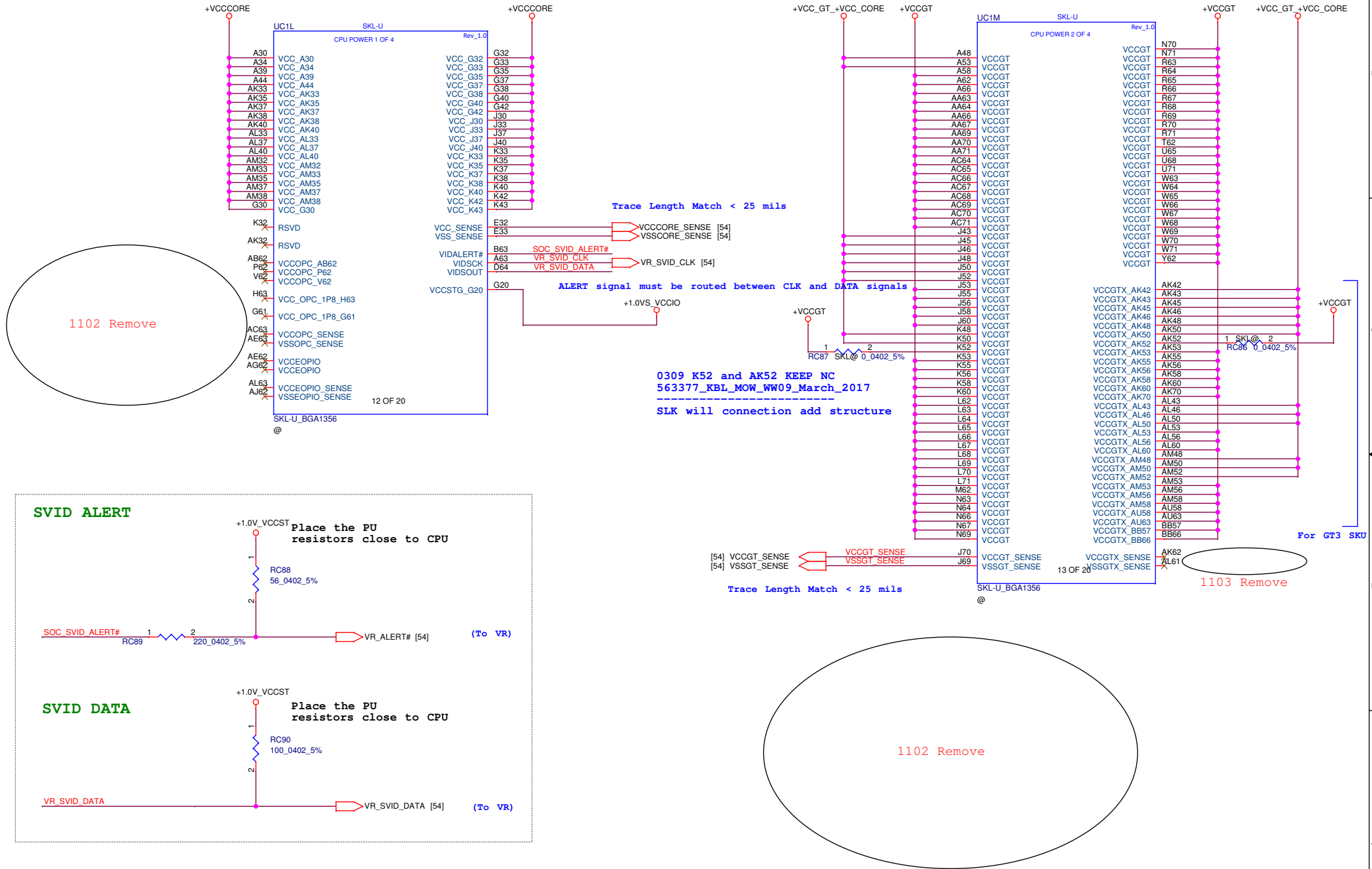
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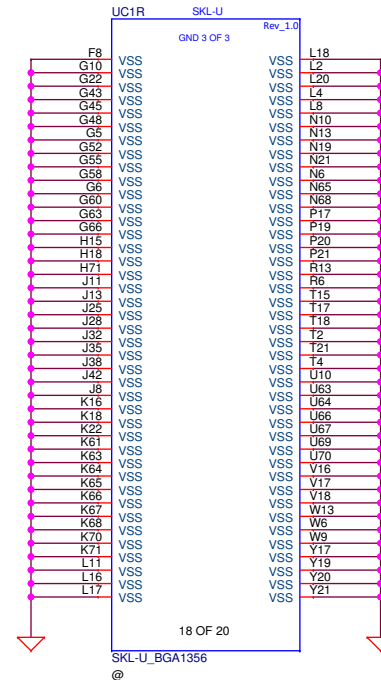
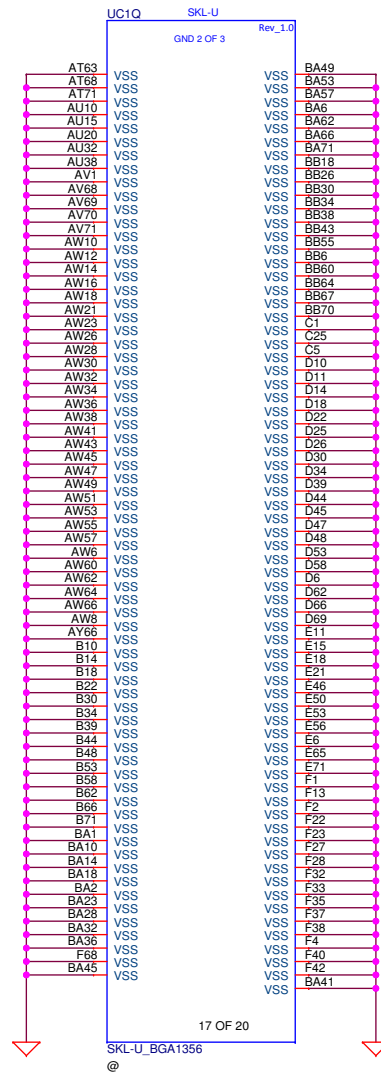
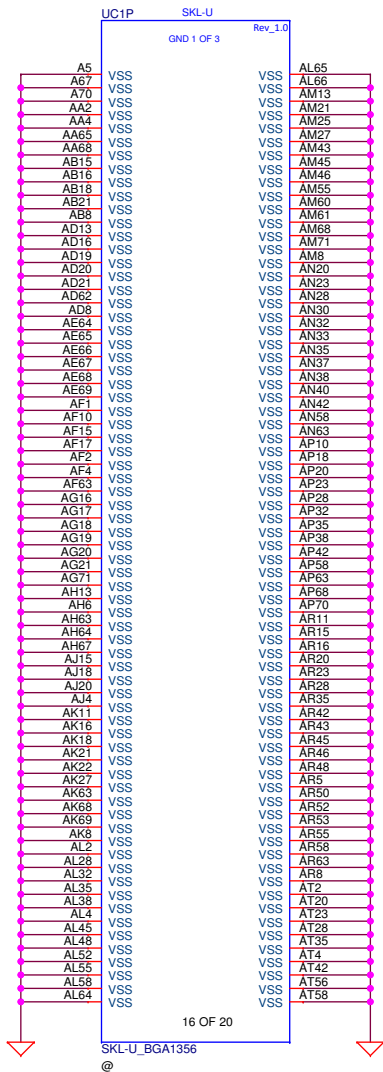
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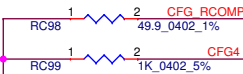
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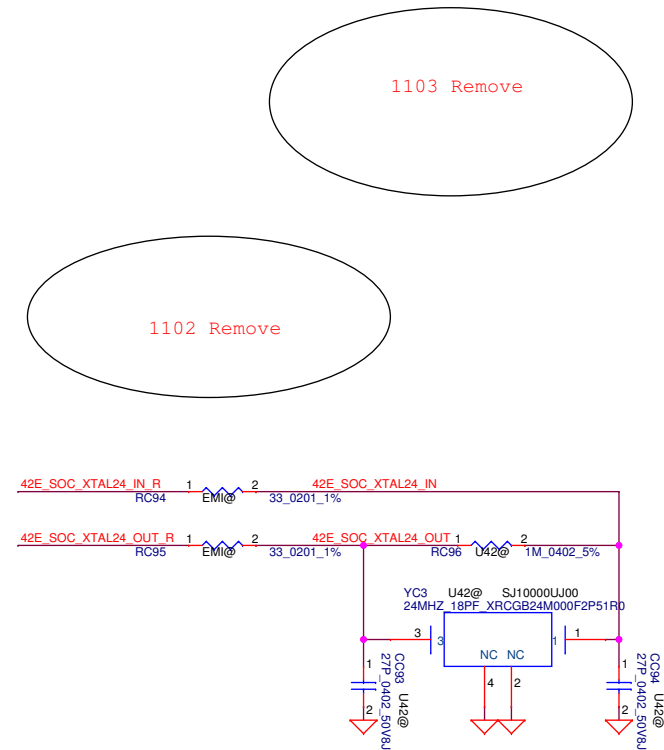
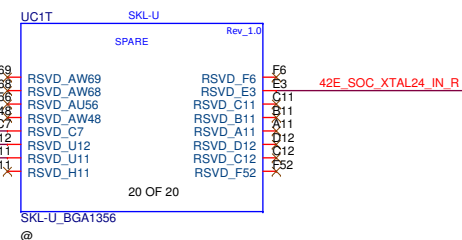
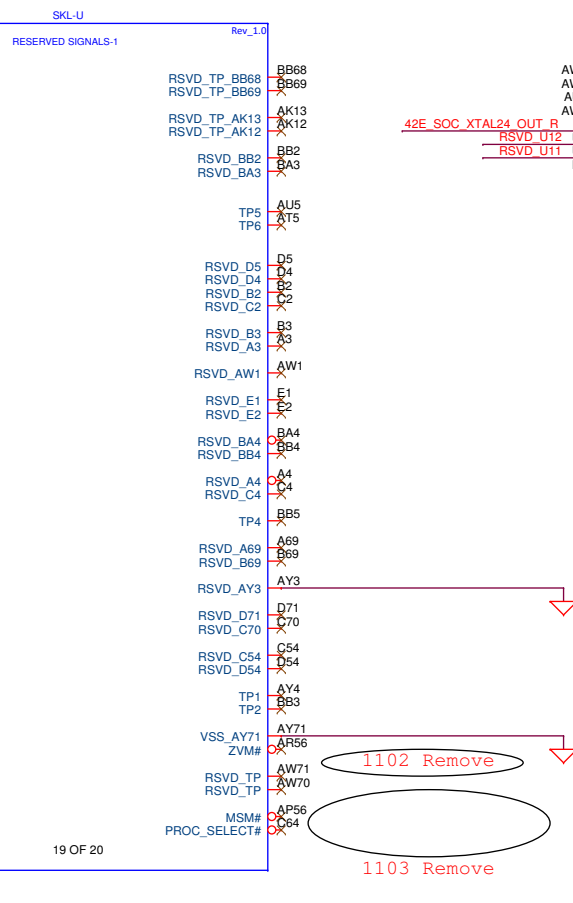


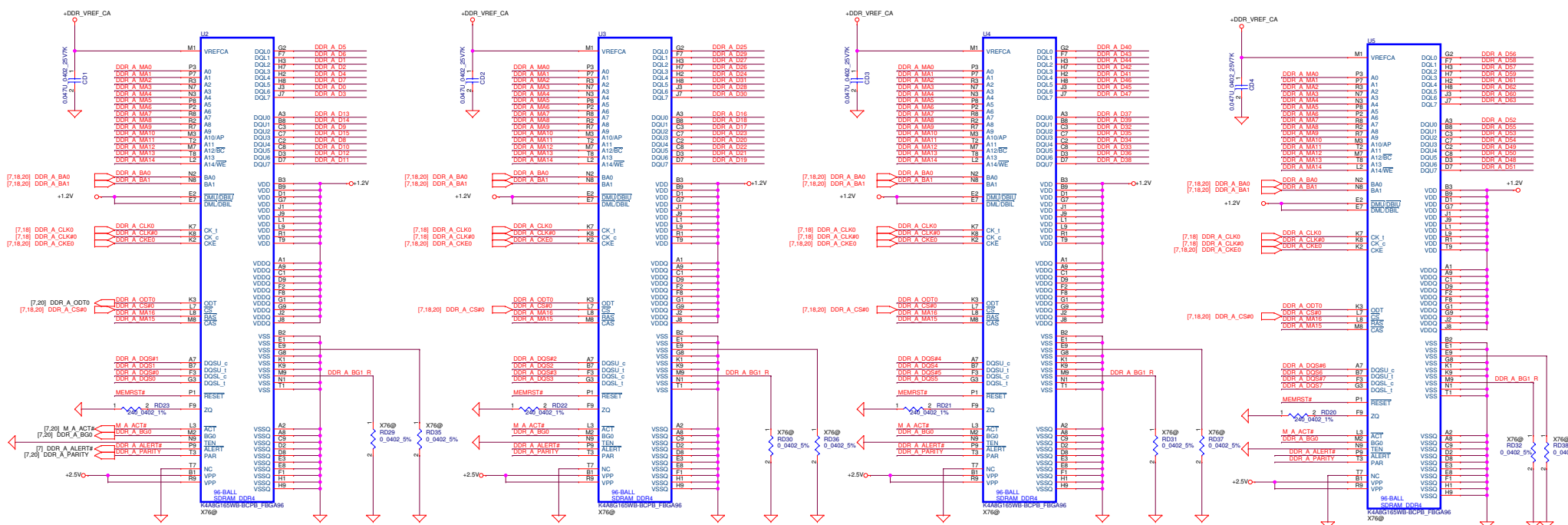
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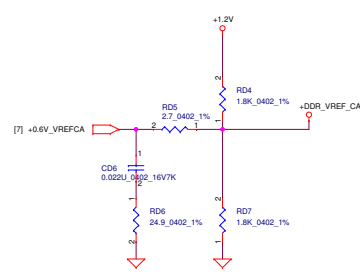
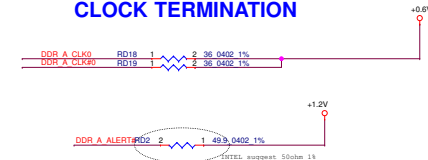


Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>





# CLOCK TERMINATION

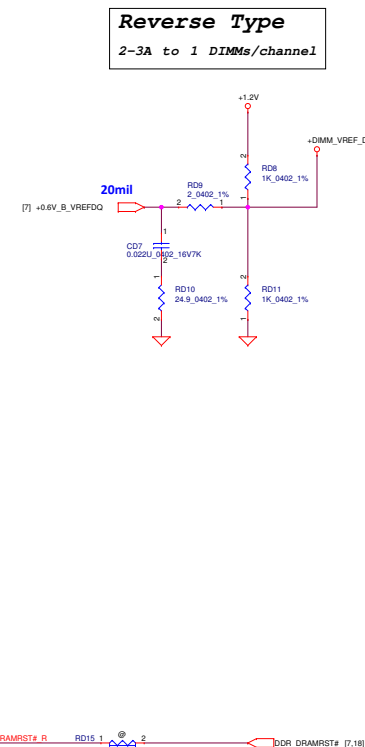
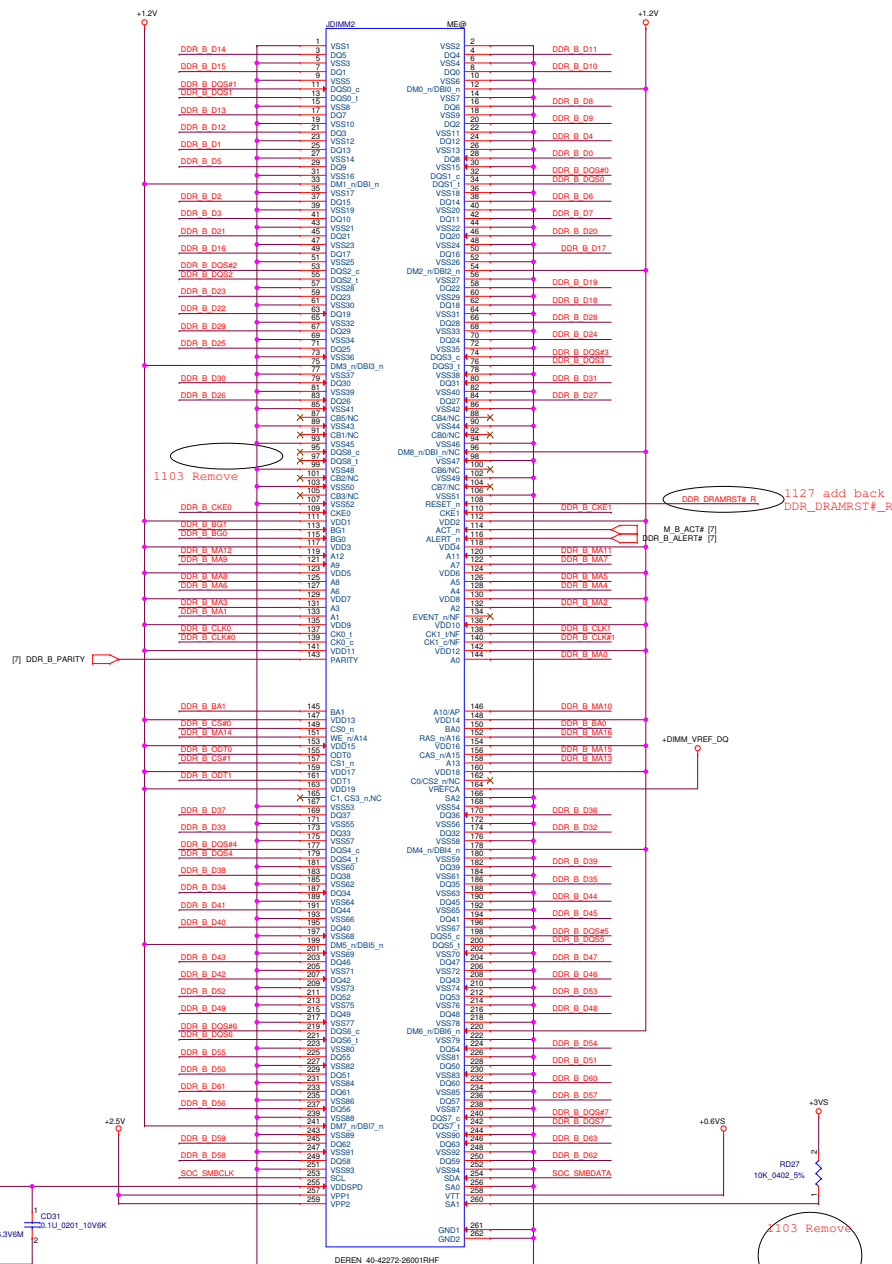
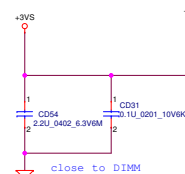
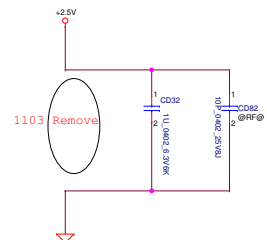
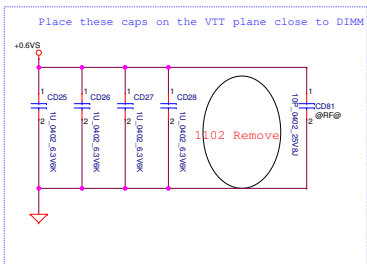
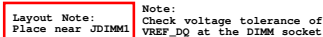


# Data mapping

U2	DQ	U3	DQ	U4	DQ	U5	DQ
DQ0	D3	DQ0	D19	DQ0	D35	DQ0	D51
DQ1	D1	DQ1	D17	DQ1	D33	DQ1	D49
DQ2	D2	DQ2	D18	DQ2	D34	DQ2	D50
DQ3	D0	DQ3	D16	DQ3	D32	DQ3	D48
DQ4	D7	DQ4	D23	DQ4	D39	DQ4	D55
DQ5	D5	DQ5	D21	DQ5	D37	DQ5	D53
DQ6	D6	DQ6	D22	DQ6	D38	DQ6	D54
DQ7	D4	DQ7	D20	DQ7	D36	DQ7	D52
DQ0	D10	DQ0	D26	DQ0	D42	DQ0	D58
DQ1	D8	DQ1	D24	DQ1	D40	DQ1	D56
DQ2	D11	DQ2	D27	DQ2	D43	DQ2	D59
DQ3	D9	DQ3	D25	DQ3	D41	DQ3	D57
DQ4	D14	DQ4	D30	DQ4	D46	DQ4	D62
DQ5	D13	DQ5	D29	DQ5	D45	DQ5	D61
DQ6	D15	DQ6	D31	DQ6	D47	DQ6	D63
DQ7	D12	DQ7	D28	DQ7	D44	DQ7	D60

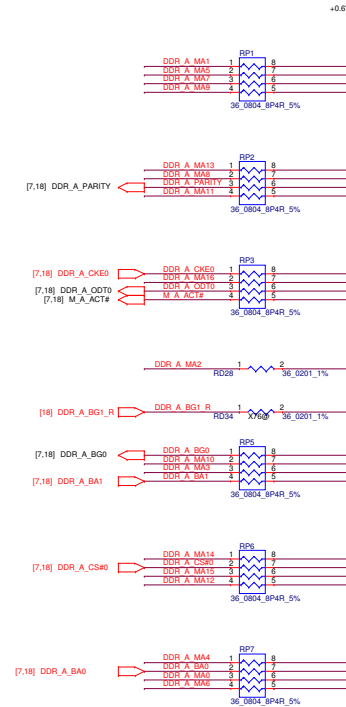
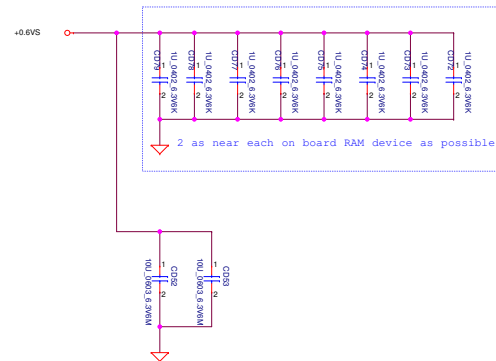
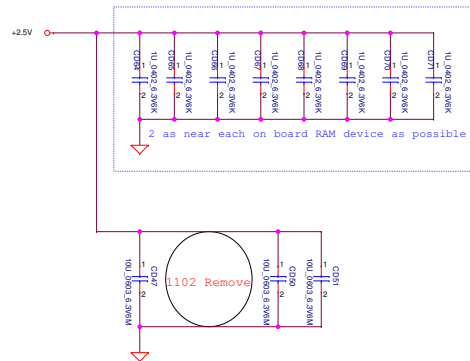
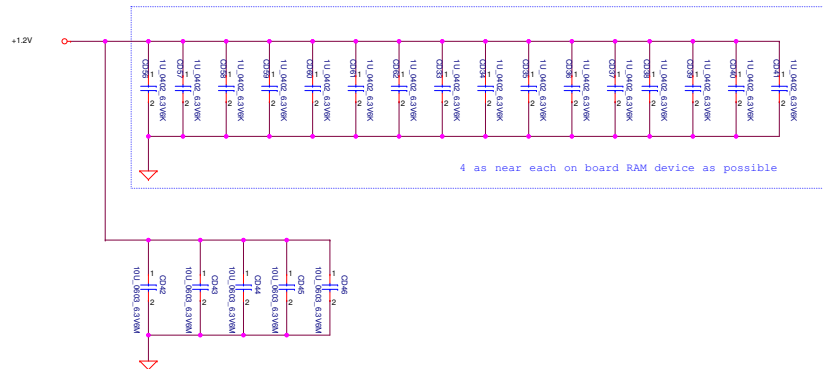
TABLE	SDP	DDP
RD29	ASM	NA
RD30	ASM	NA
RD31	ASM	NA
RD32	ASM	NA
RD33	NA	ASM
RD34	NA	ASM
RD35	0.5%	243.1%
RD36	0.5%	243.1%
RD37	0.5%	243.1%
RD38	0.5%	243.1%

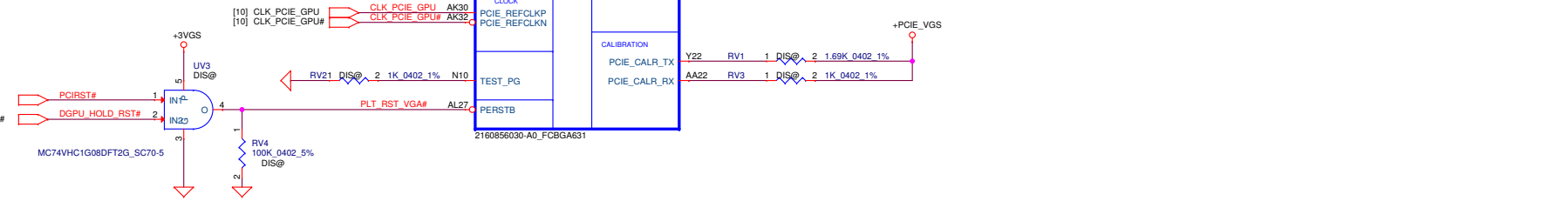
LOGIC



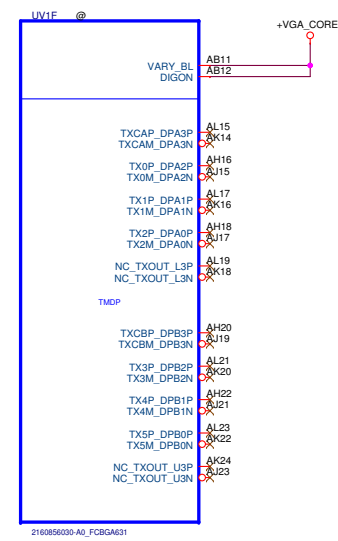
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[7:18] DDR\_A\_MA[0:16]





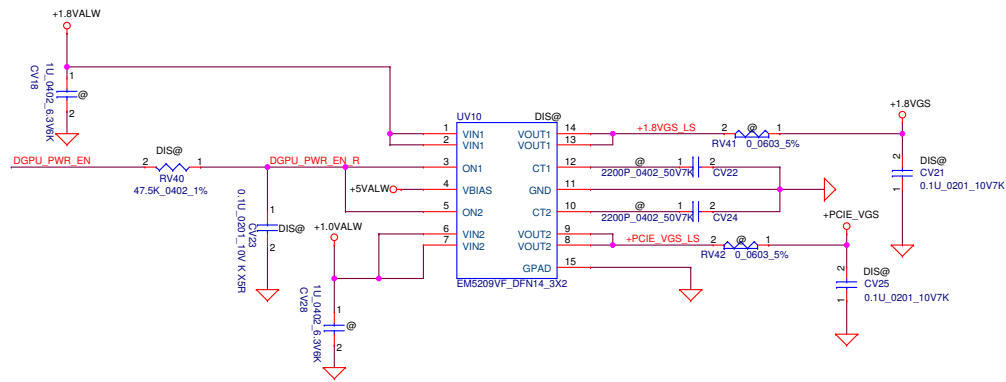
No Use GPU Display Port output



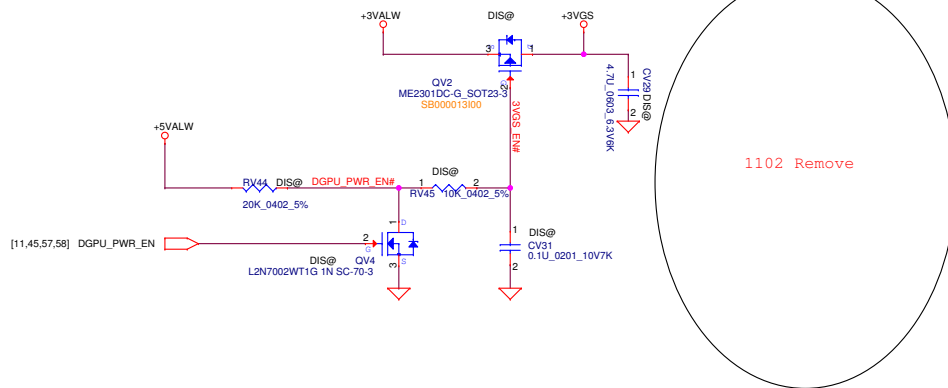
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Issued Date	2017/08/02	Deciphered Date	2018/08/02	Title	M30/M70_PCIE/DP
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				Date	LA-F486P
				Sheet	21 of 66



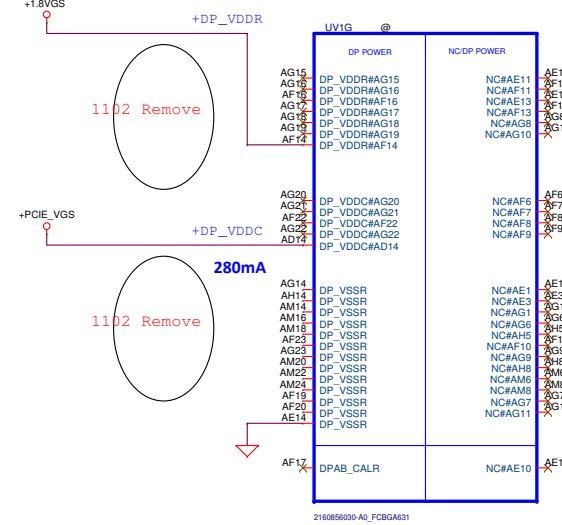
**+1.8VALW TO +1.8VGS  
+1.0VALW TO +PCIE\_VGS  
Load switch**



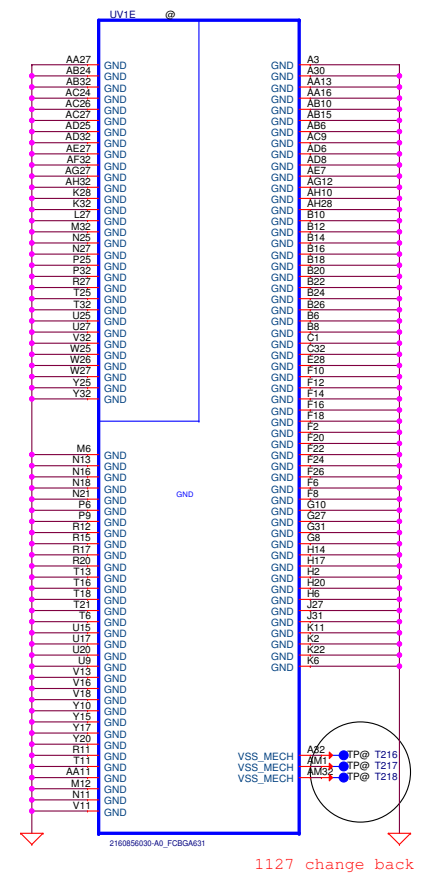
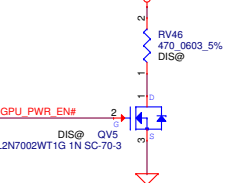
**+3VALW to +3VGS**



**No Use GPU Display Port output**



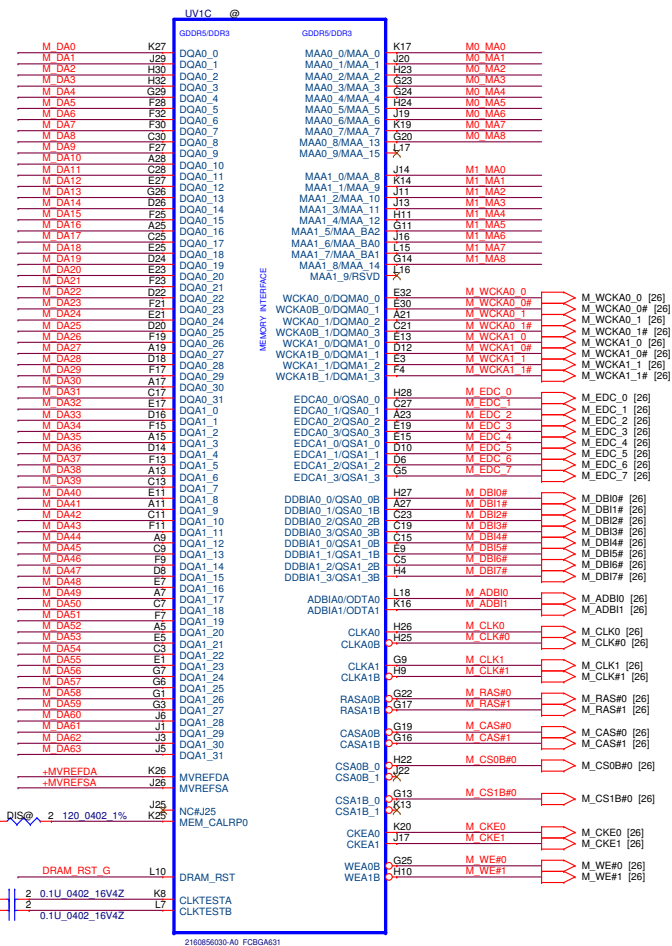
**+VGA\_CORE**



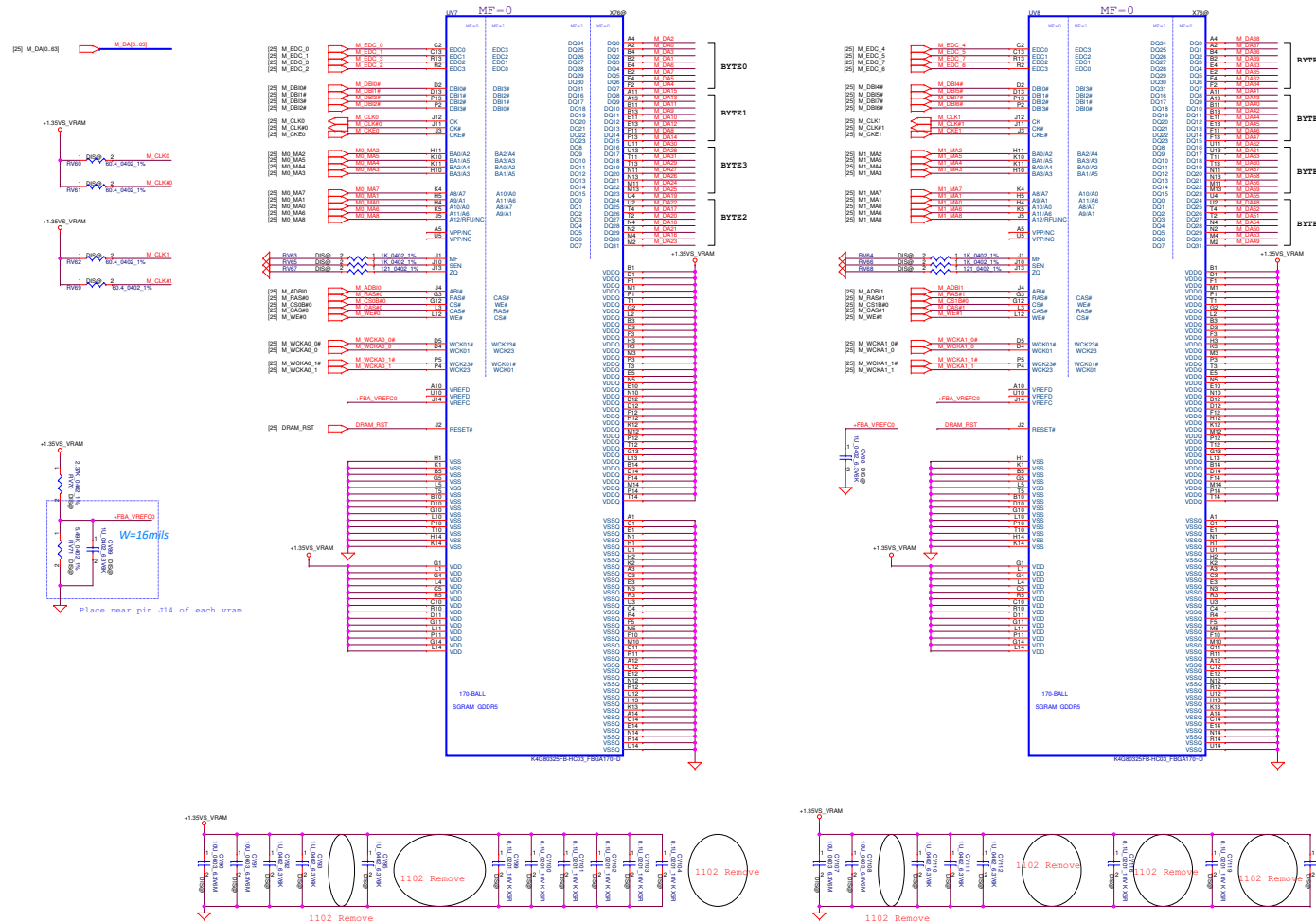
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				Rev	0.3





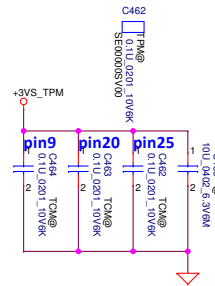


## Memory Partition A



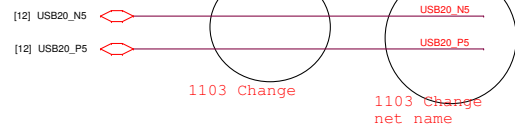
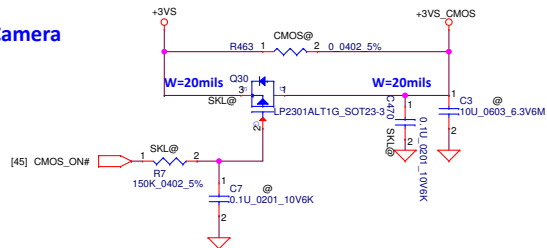
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			DATE	17/08/02
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10

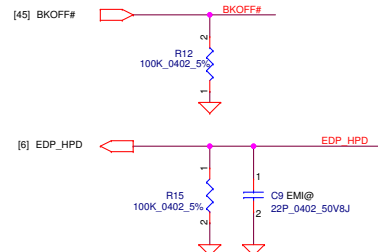
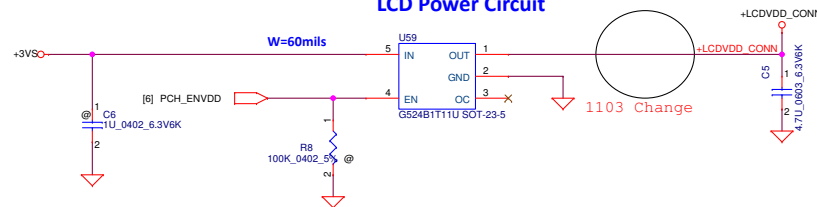


Nati onzInfi neon TCM TPM			Nati onzInfi neon TCM TPM		
Pin1	NC	VDD	Pin17	NC	NC
Pin2	NC	GPIO	Pin18	LRESET#	LRESET#
Pin3	NC	NC	Pin19	LAD3	LAD3
Pin4	NC	NC	Pin20	VDD	VDD
Pin5	NC	NC	Pin21	LAD2	LAD2
Pin6	NC	NC	Pin22	LCLK	LCLK
Pin7	NC	NC	Pin23	LFRAME#	LFRAME#
Pin8	NC	NC	Pin24	LAD1	LAD1
Pin9	VDD	VDD	Pin25	VDD	VDD
Pin10	NC	VDD	Pin26	GND	GND
Pin11	GND	NC	Pin27	LAD0	LAD0
Pin12	NC	NC	Pin28	NC	SERIRQ
Pin13	NC	NC	Pin29	NC	NC
Pin14	NC	NC	Pin30	NC	NC
Pin15	NC	GND	Pin31	NC	PP
Pin16	GND	GND	Pin32	GND	GND

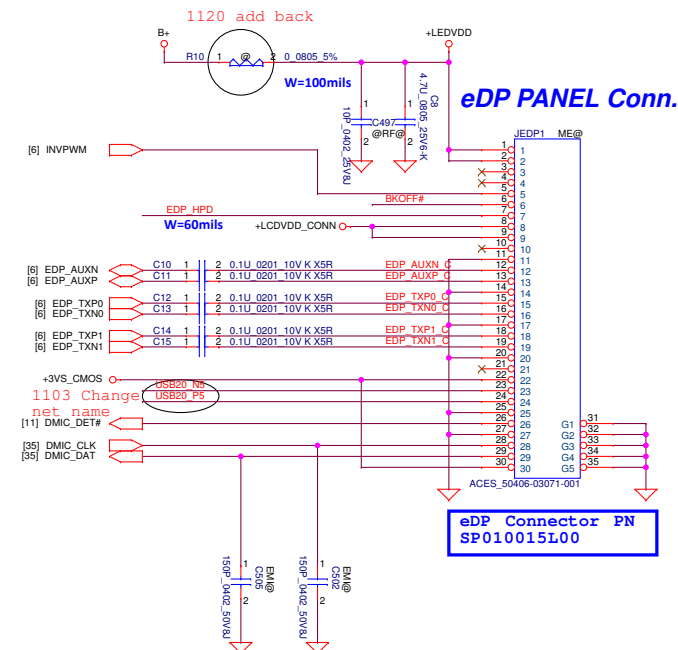
## Camera



## LCD Power Circuit

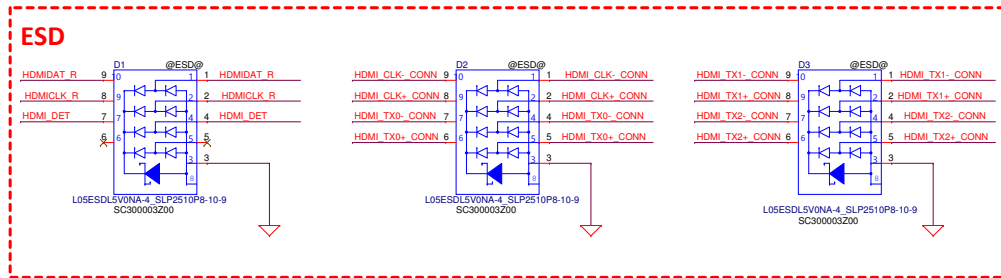
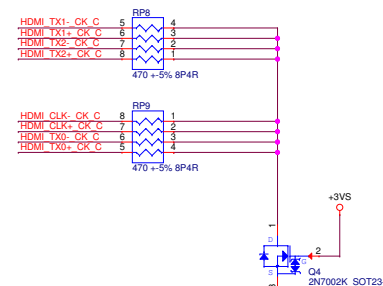
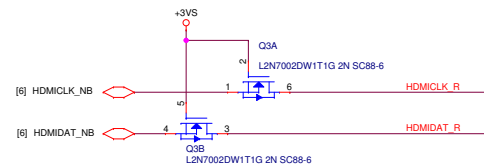
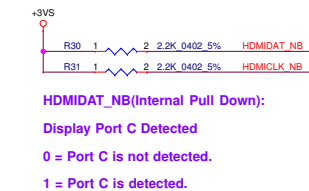
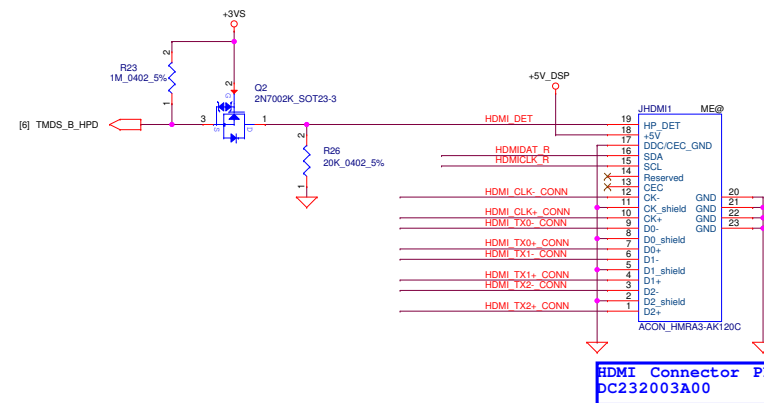
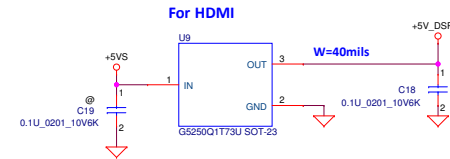
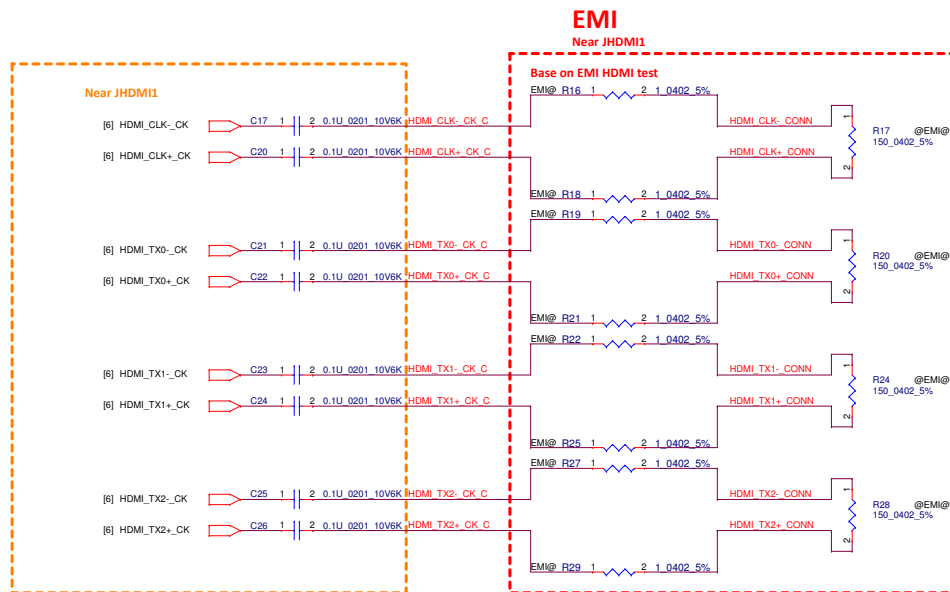


eDP  
Camera

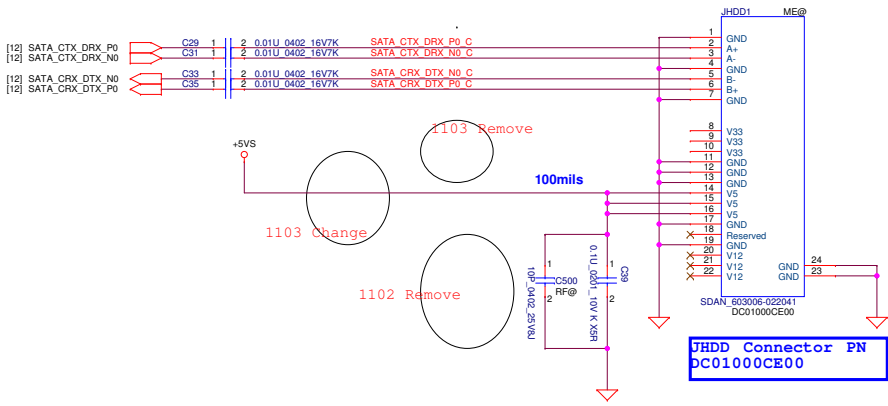


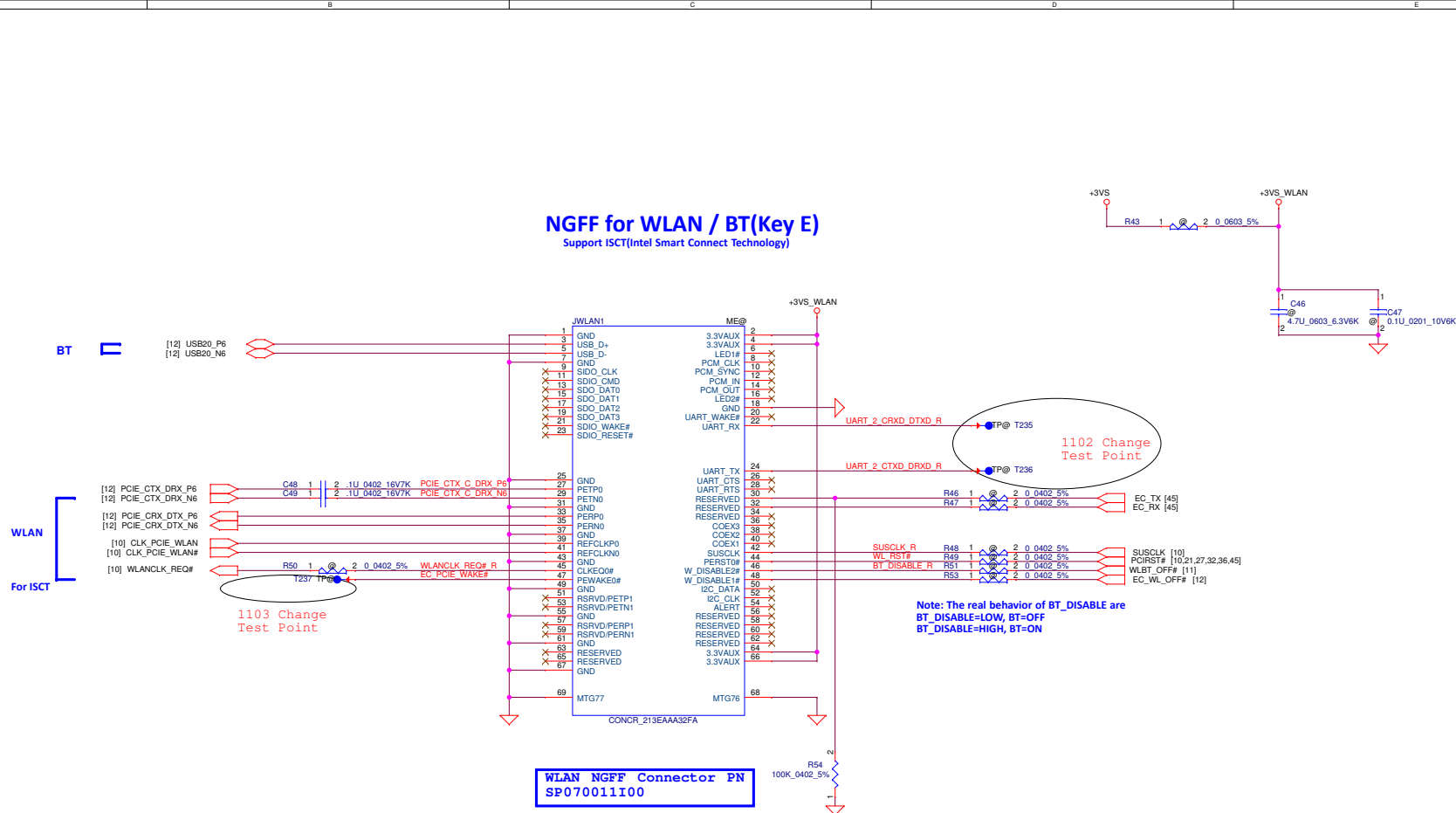
eDP Connector PN  
SP010015L00

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## 6.2. NGFF Module Pin outs

The following section incorporates a series of NGFF module side pin outs covering the different Slots. Because some signals have directionality associated with them, their names and locations may be different between the Platform side and the Module side.

Please note the main differences between Platform side pin outs and Module side pin outs as seen in the diagram below:

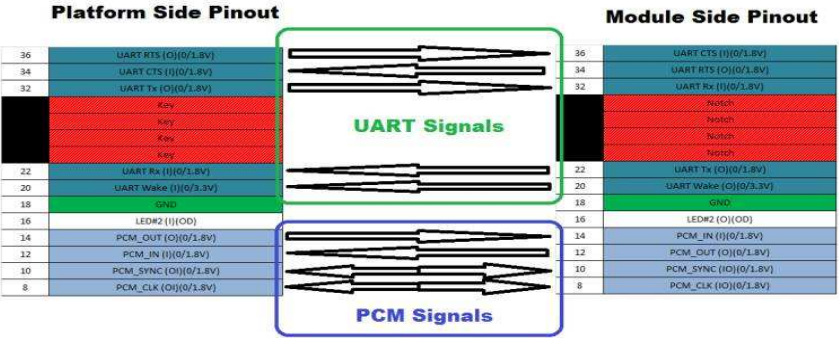
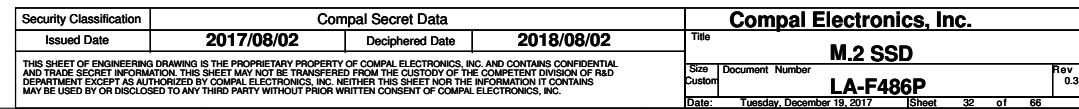


Figure 6-1: UART & PCM Signal Direction & Signal Name Changes

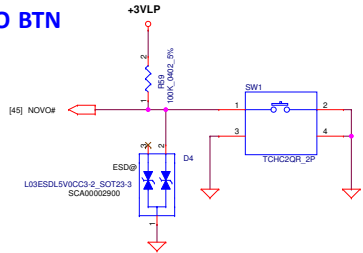
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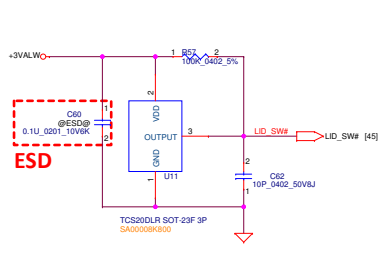




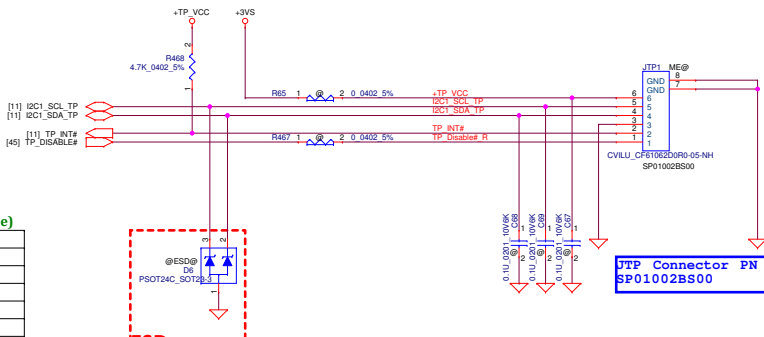
NOVO BTN



LID



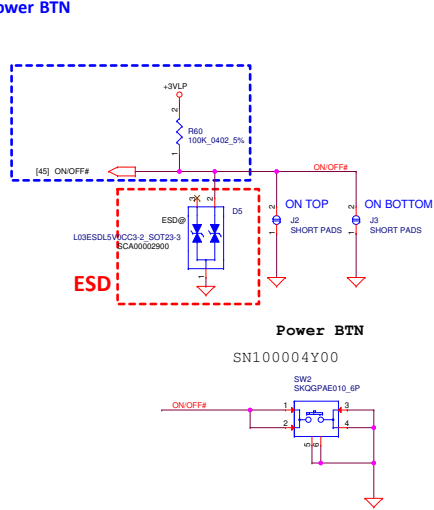
ClickPad



Click Pad Pin define(Module)

Pin1	VDD_3.3V
Pin2	SCL
Pin3	SDA
Pin4	GND
Pin5	INT
Pin6	LID CLOSE

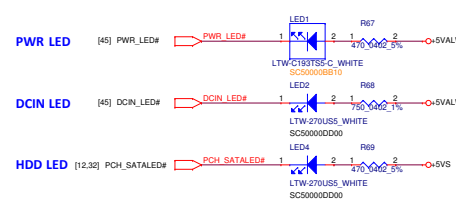
Power BTN



Charge LED

+5VL 1214 change PWR source

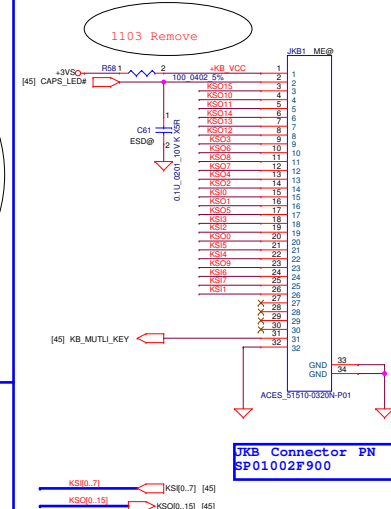
LED



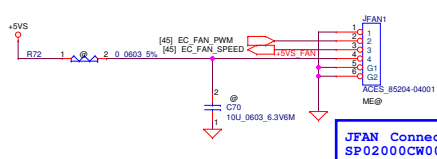
WHITE

P/N:SC500007F00

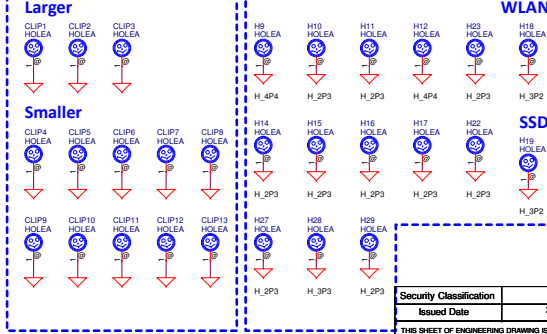
KB



FAN Conn



Shielding Clip



WLAN

Thermal

SSD

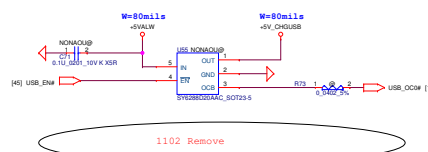
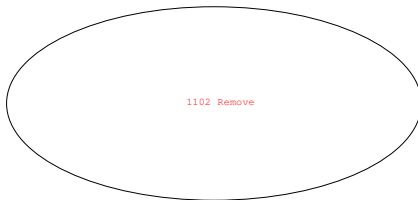
LAN

NPTH

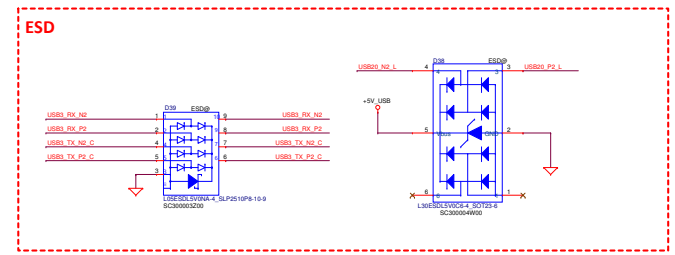
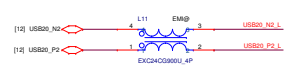
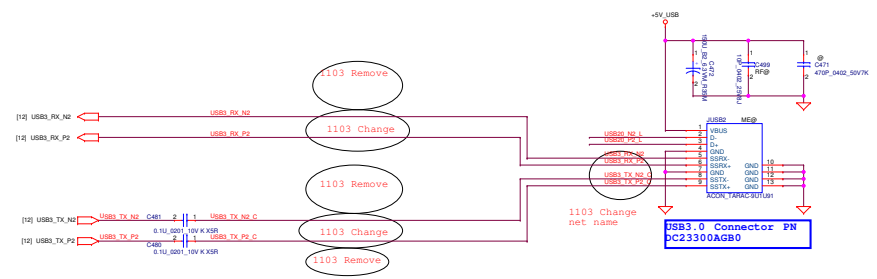
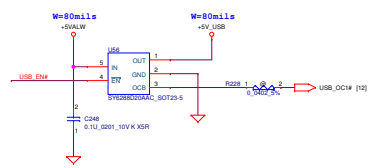
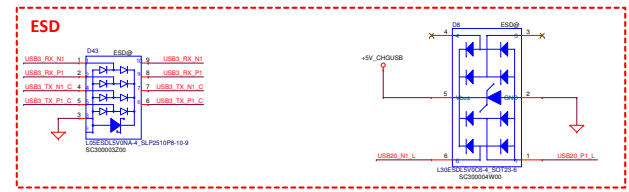
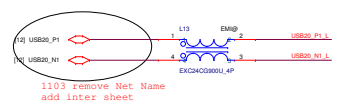
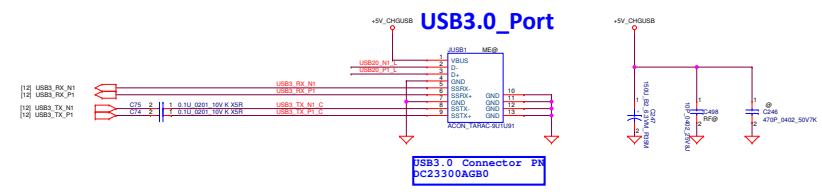
CPU

VGA

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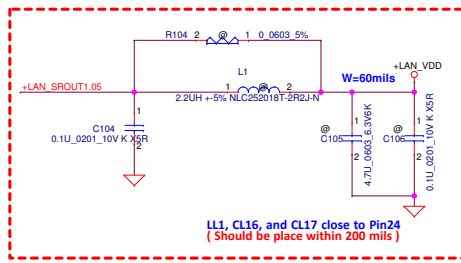
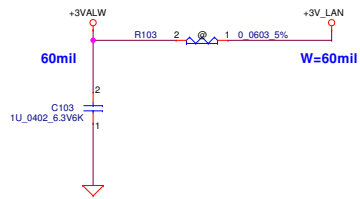


1102 Remove



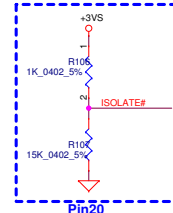
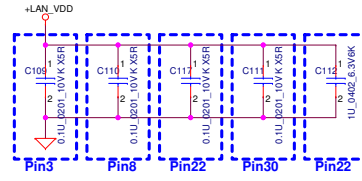
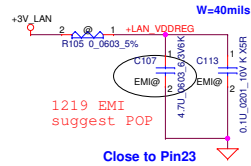
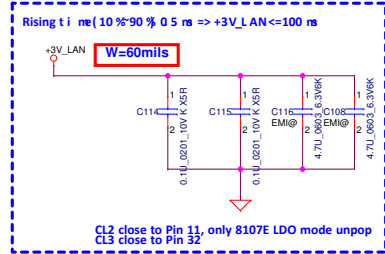
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Change	Change	
Date	Version	1.0



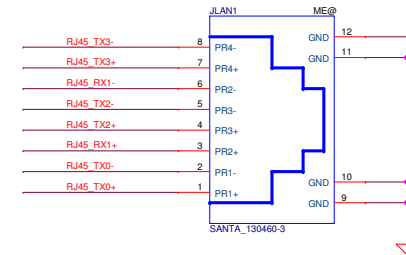


	1.0V Source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
RTL8111H	LDO	X	X	X	O	O

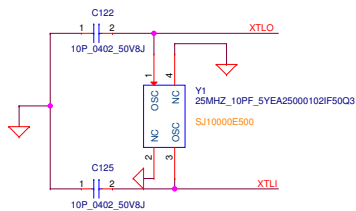
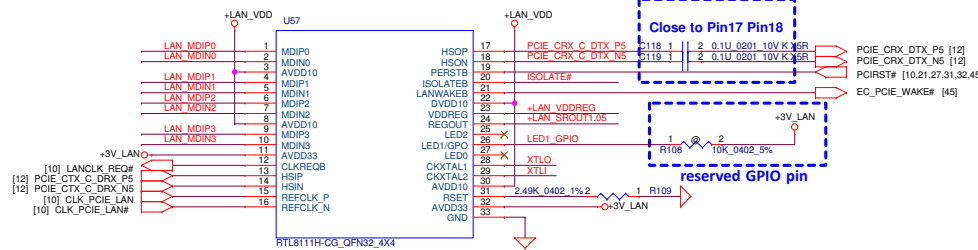
Please refer to the table above when using different 1.0V supply source.



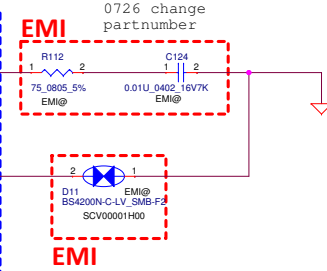
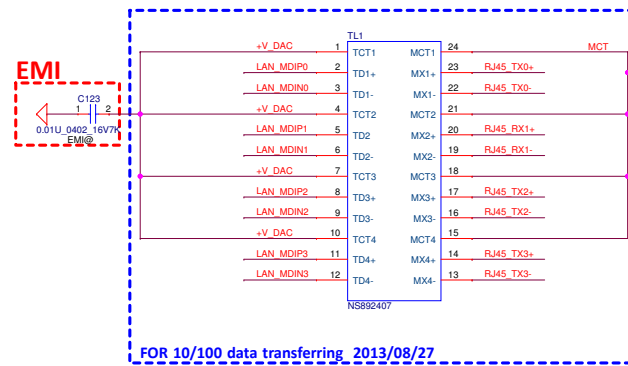
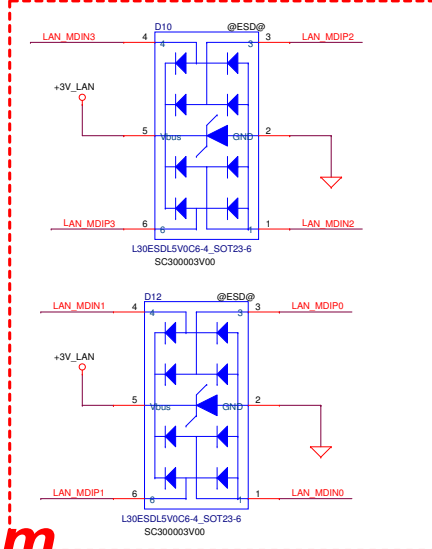
## RJ-45 CONN.



LAN Connector PN  
PC23400DP00

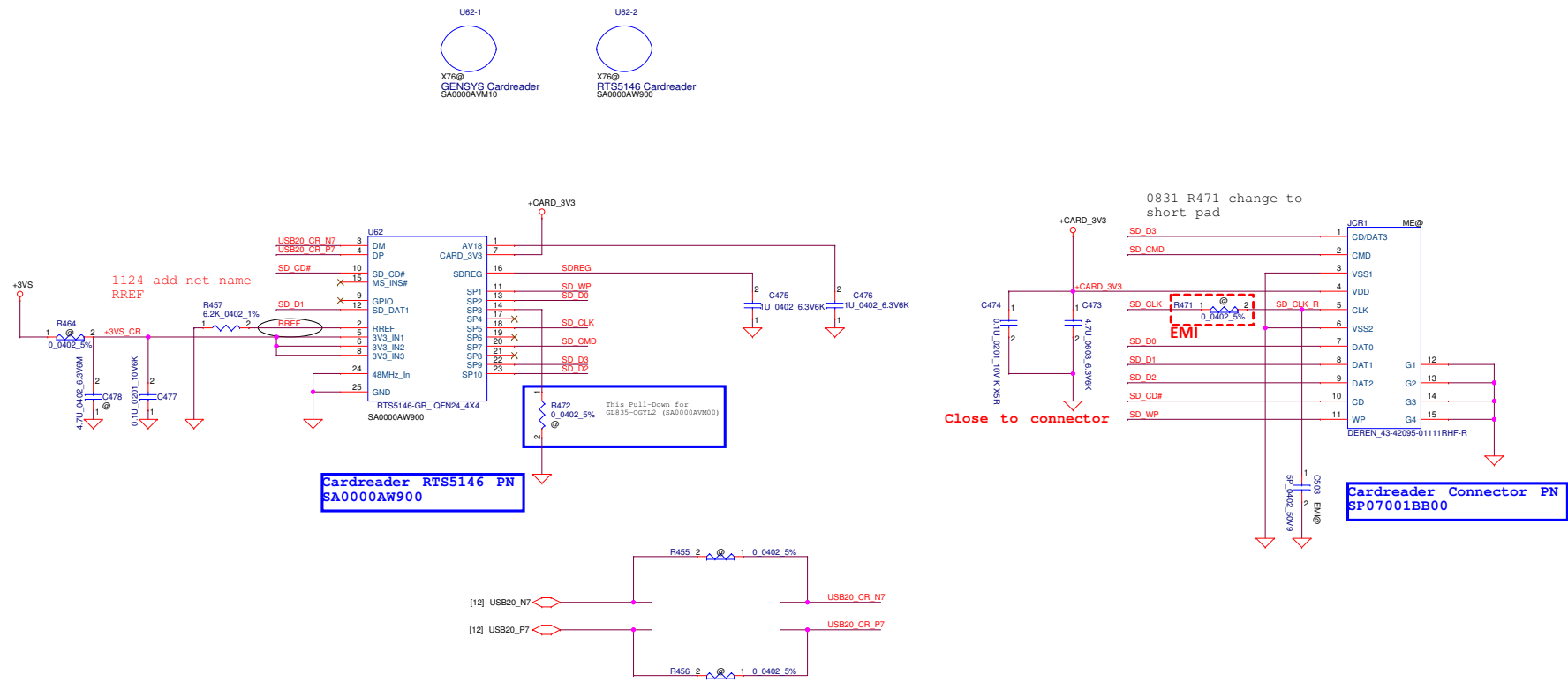


## ESD



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Issued Date	2017/08/02	LAN RTL8111H
Deciphered Date	2018/08/02	LAN F486P
Size	Document Number	Rev 0.3
C	Size	Rev 0.3
Date	Tuesday, December 19, 2017	Sheet 36 of 66

## Card Reader

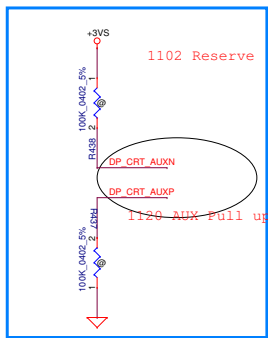


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				Custom	LA-F486P	0.3
				Date:	Tuesday, December 19, 2017	Sheet 37 of 66

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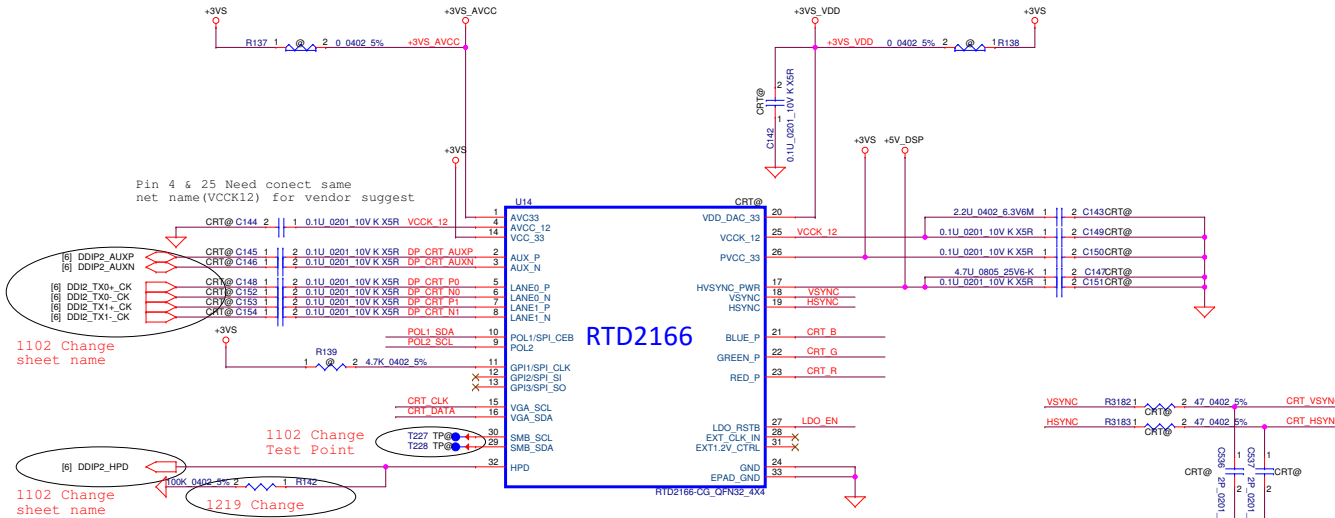
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DDPB\_AUXP  
DDPB\_AUXN

Use a 75~200 nF AC coupling capacitor between the PCH and the connector.  
Intel recommends having a pull-up resistor of 100 KΩ on AUXN and 100 KΩ pull-down on AUXP between the AC capacitor and the connector, to assist source detection by the sink device.

1120 AUX Pull up/down reserve modify after cap

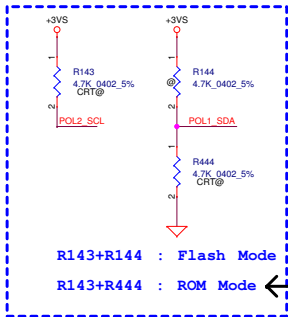


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Test Point

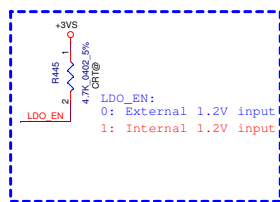
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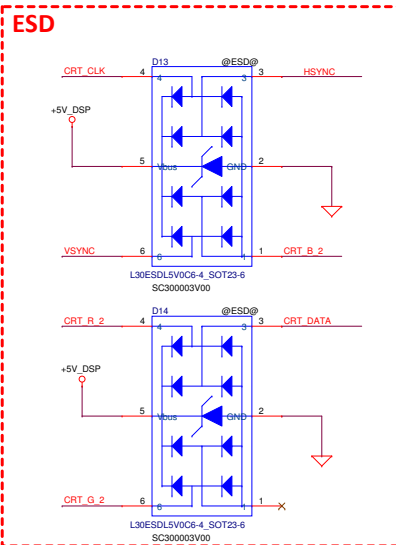


R143+R144 : Flash Mode  
R143+R444 : ROM Mode

Default

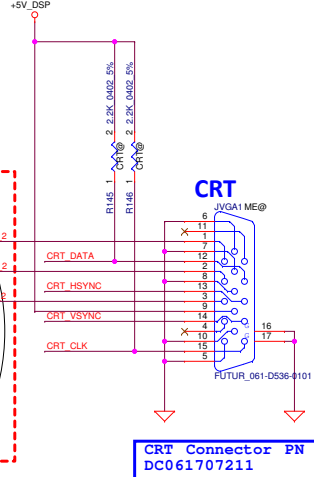
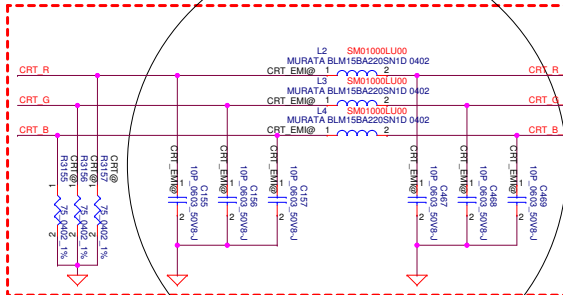


LDO\_EN:  
0: External 1.2V input  
1: Internal 1.2V input



EMI

1215 define structure



CRT Connector PN  
DC061707211

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Date: Tuesday, December 19, 2017		Sheet		39	of 66

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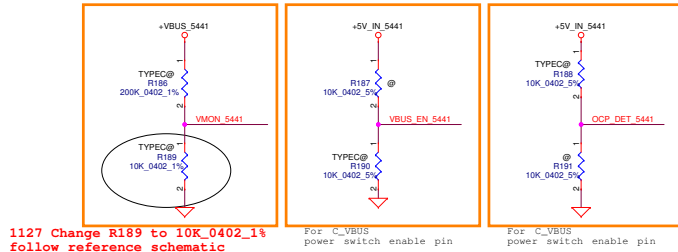
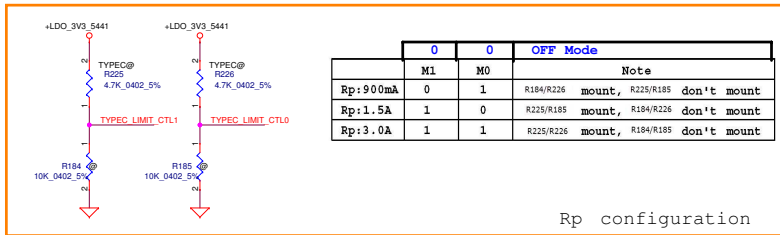
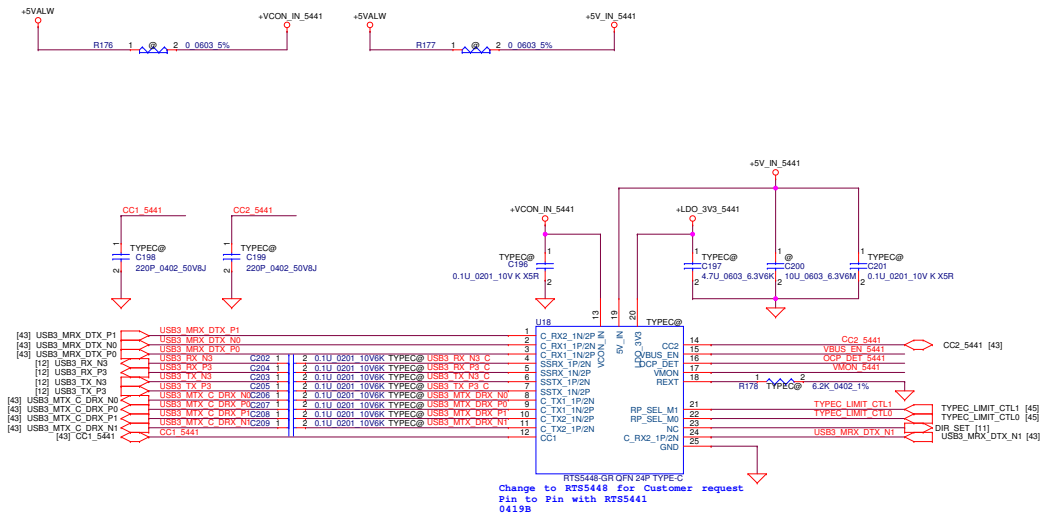
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				LA-F486P	
				Date: Tuesday, December 19, 2017	
				Sheet	40 of 63



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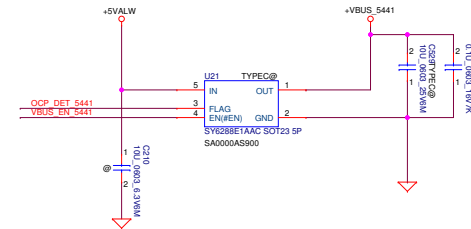
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Date: Tuesday, December 19, 2017		Sheet 41 of 66			



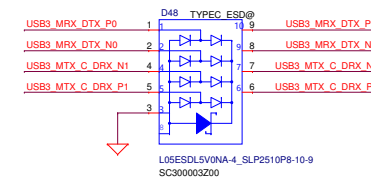
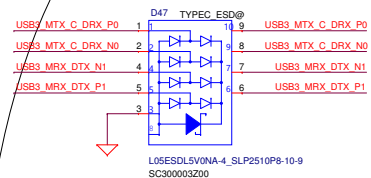
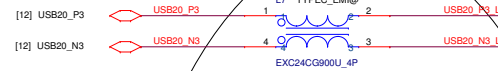
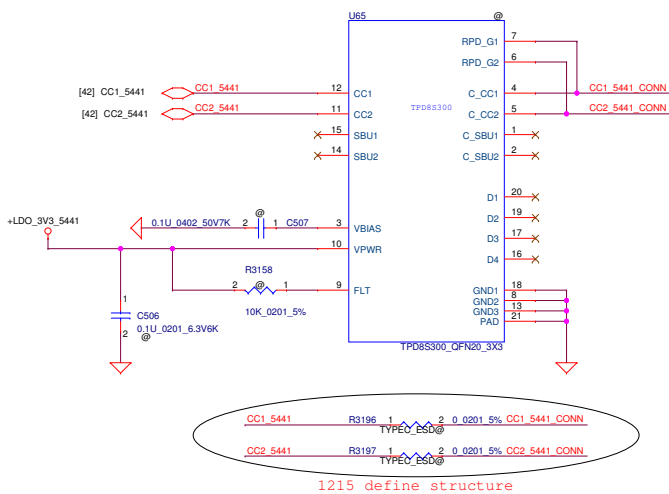
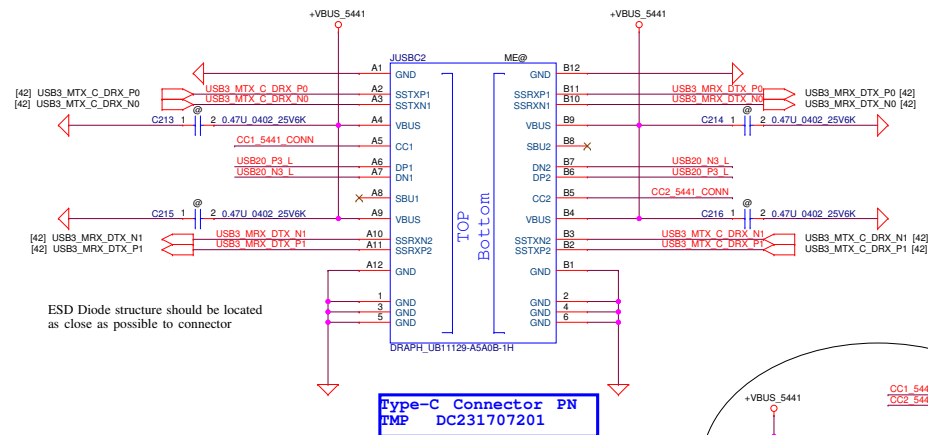
Power switch enable pin	Note	
Low Active	R190/R187 mount	Pull Up & Down
High Active	R190 mount, R187 don't mount	Pull Down

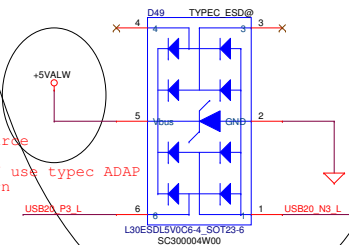
Power switch OCP pin	Note	
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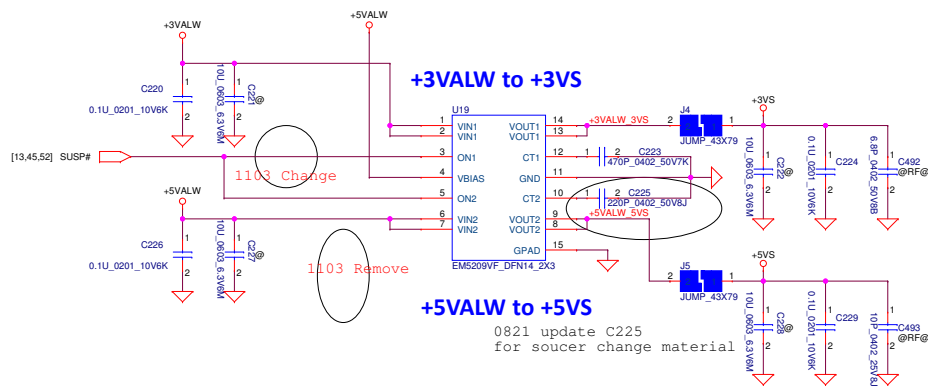


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Size	Document	Number	Rev	0.3
Custom	LA-F486P			
Date:	Tuesday, December 19, 2017	Sheet	42	of 63

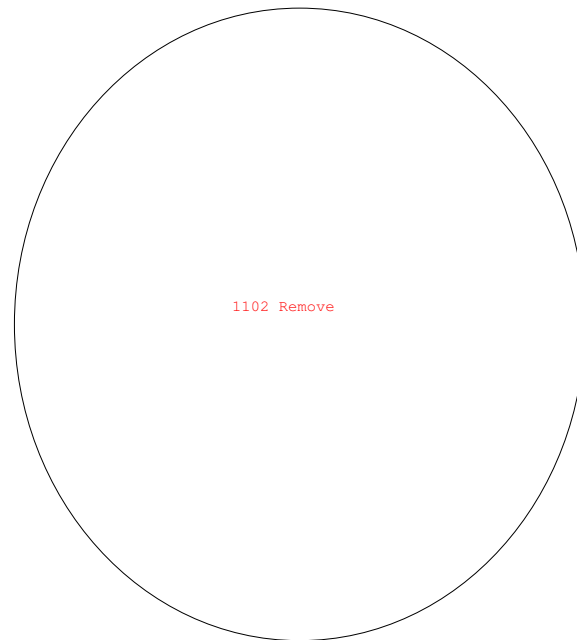
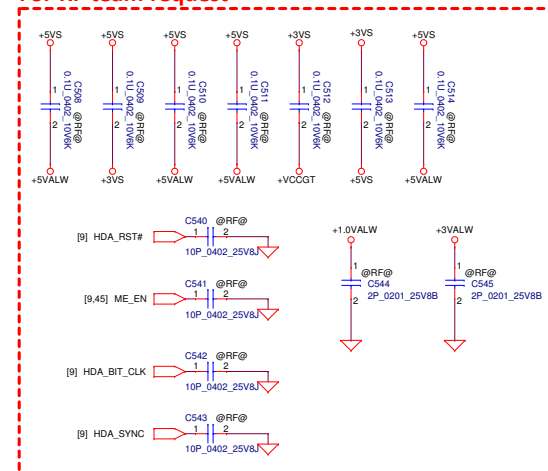


ESD for USB20 Lines and Control lines

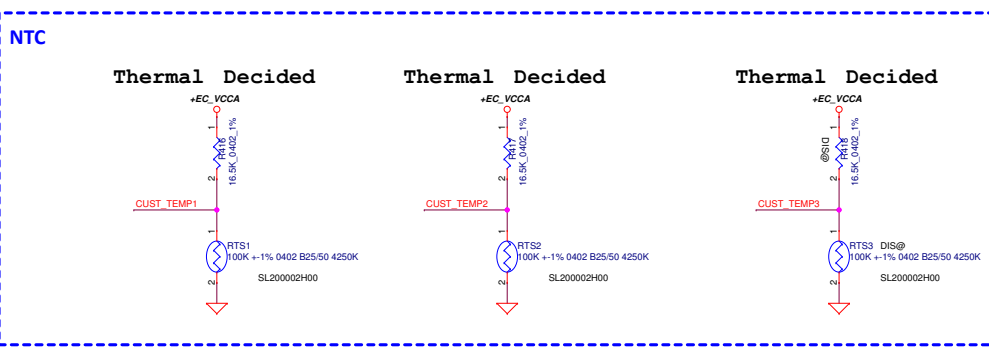




### For RF team request

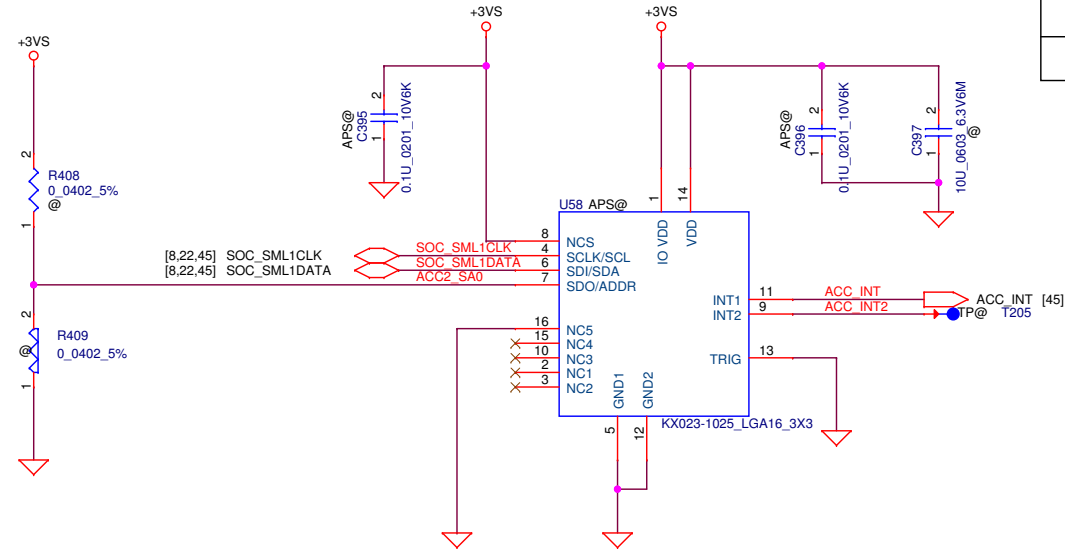


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Size		Document Number		Rev	
C		LA-F486P		0.3	
Date:		Tuesday, December 19, 2017		Sheet 44 of 66	

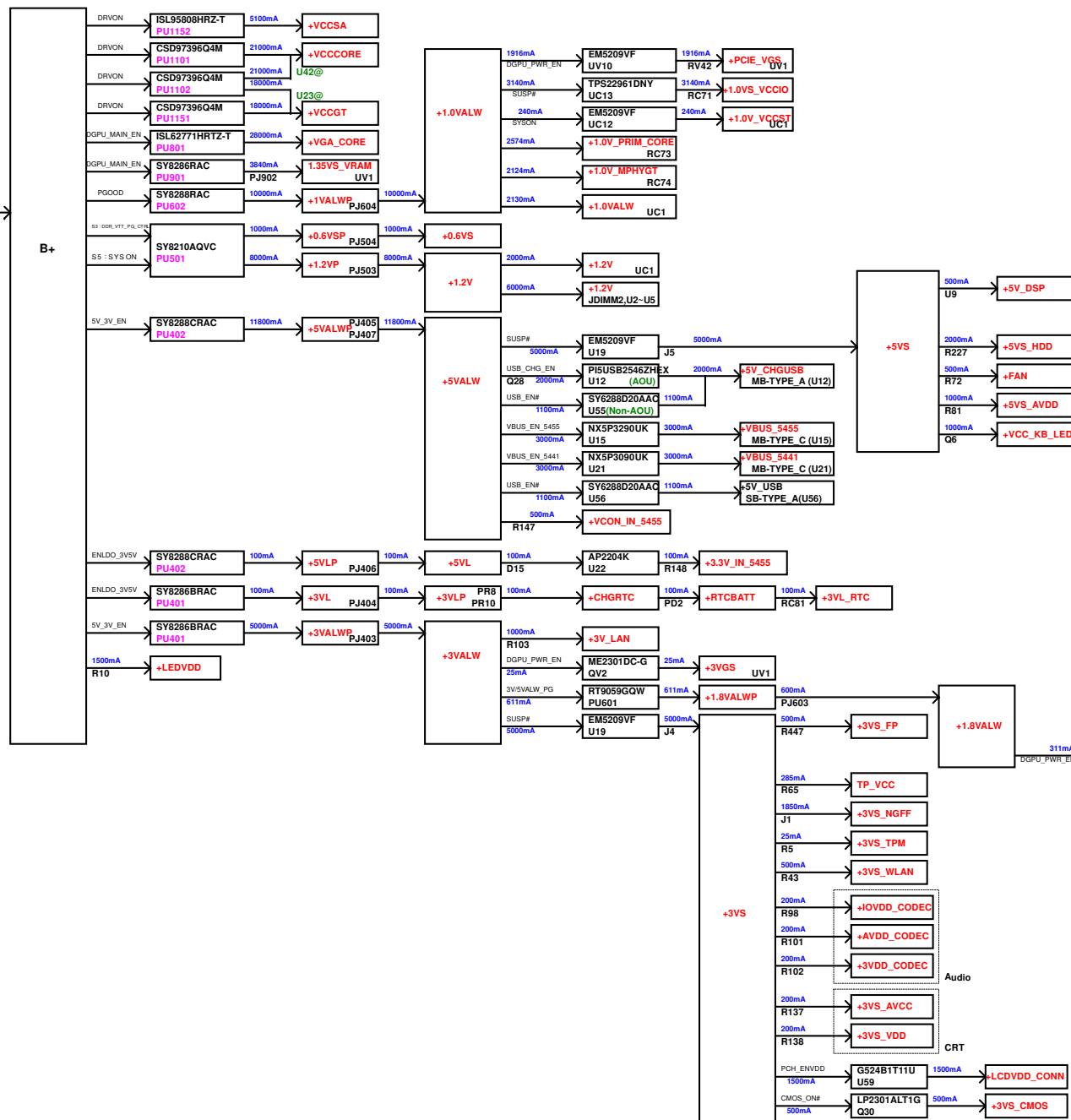


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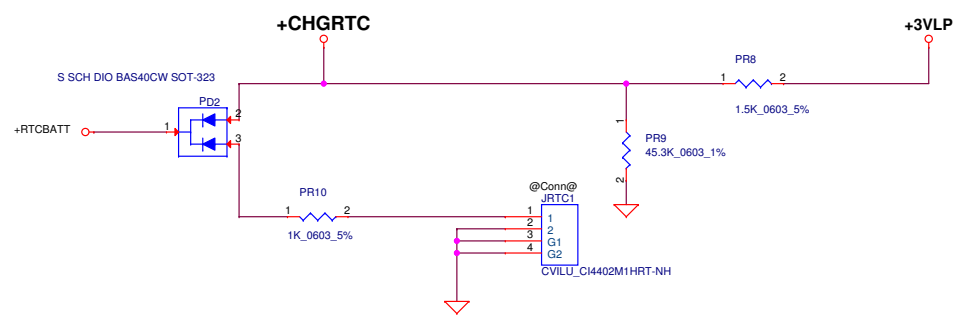
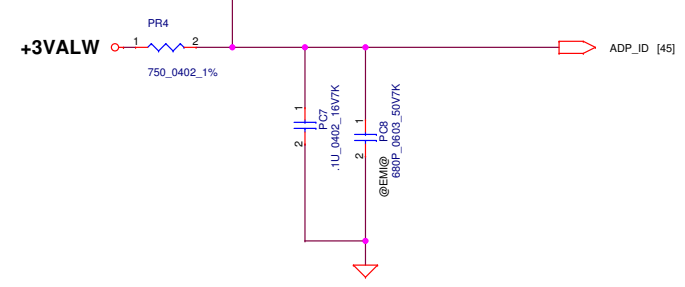
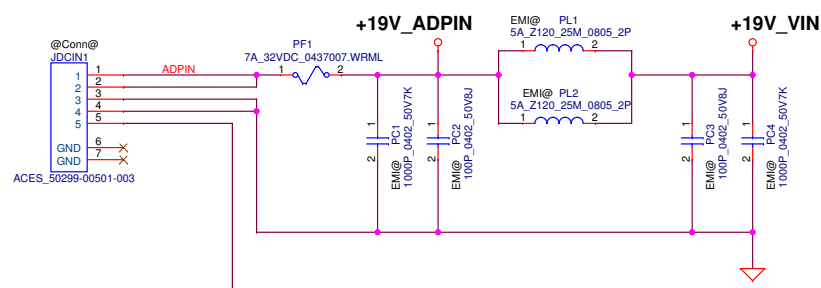
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<b>VDD</b>	3Fh/3Eh
<b>VSS</b>	3Dh/3Ch



**WWW.AliSaler.Com**



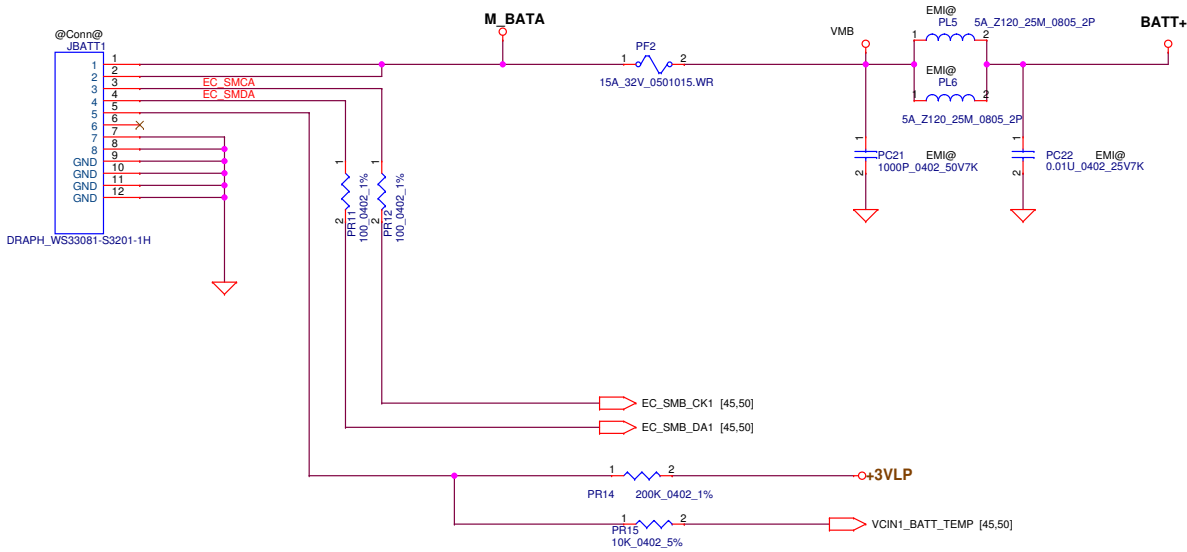
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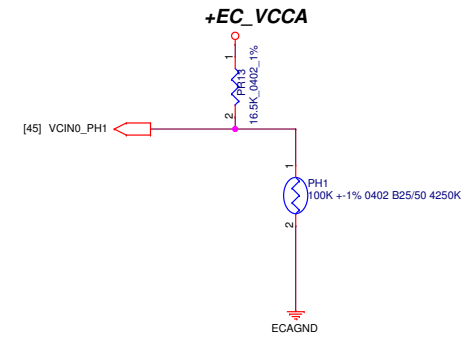
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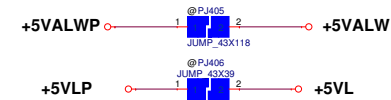
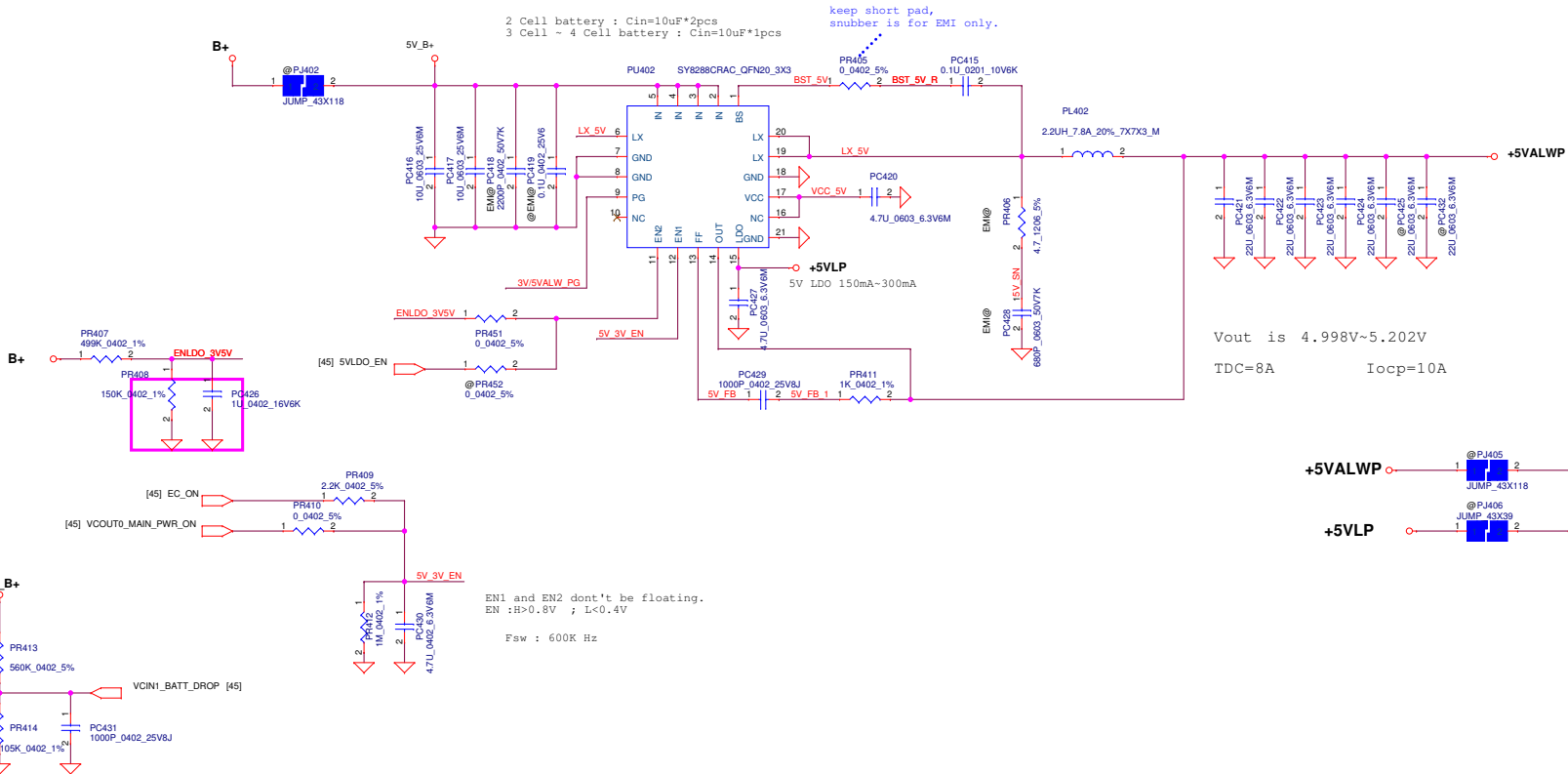
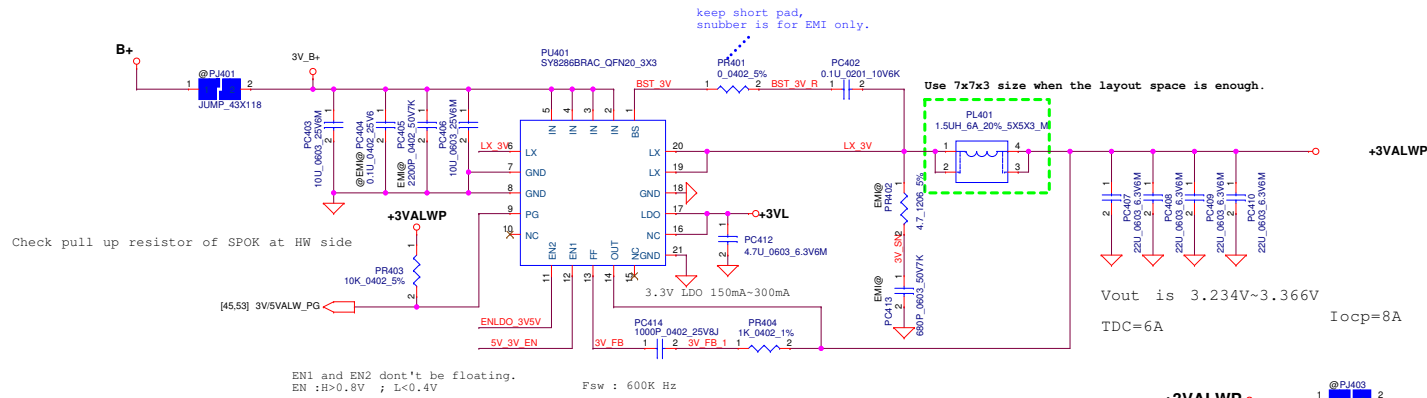


**PH201 under CPU bottom side :**  
**CPU thermal protection at 93 +-3 degree C**  
**Recovery at 56 +-3 degree C**

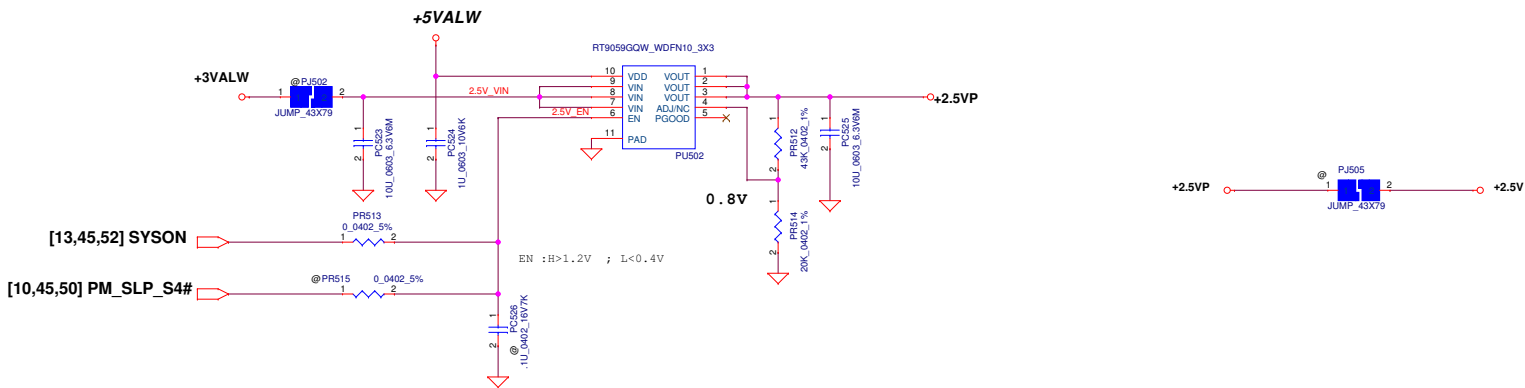
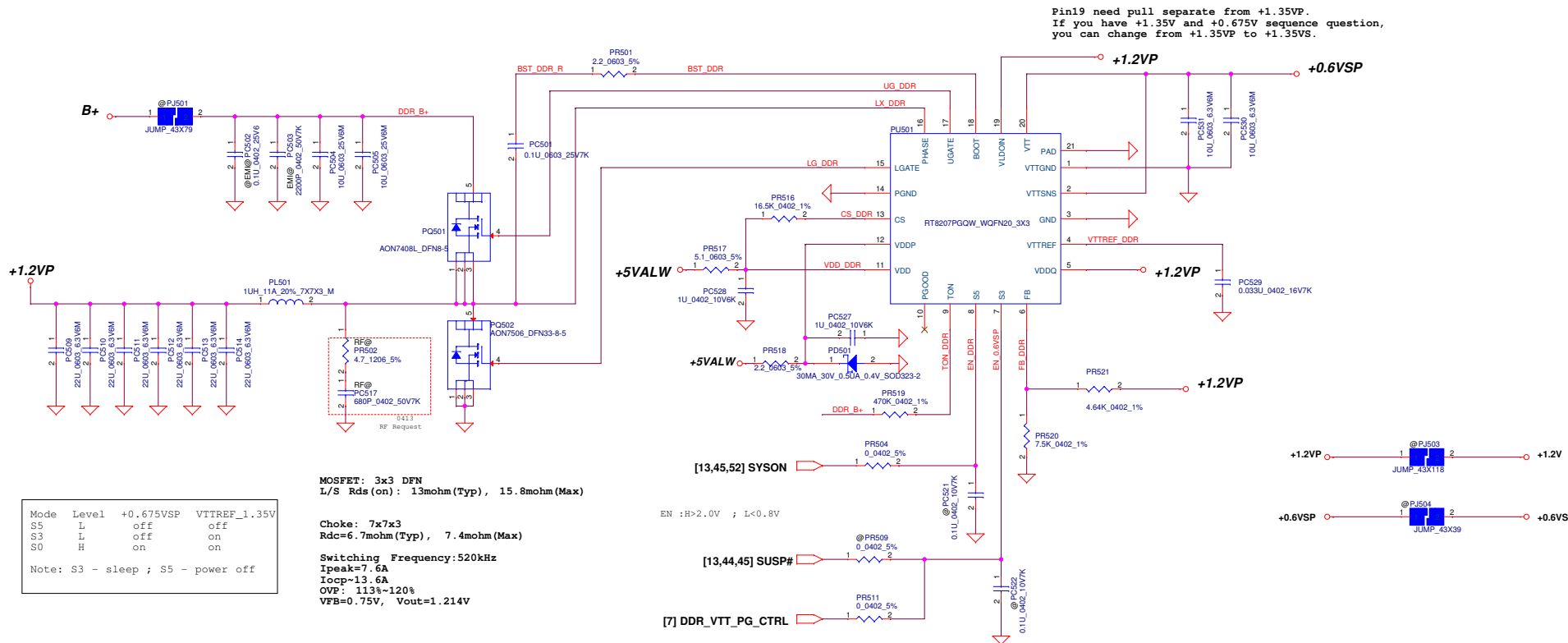


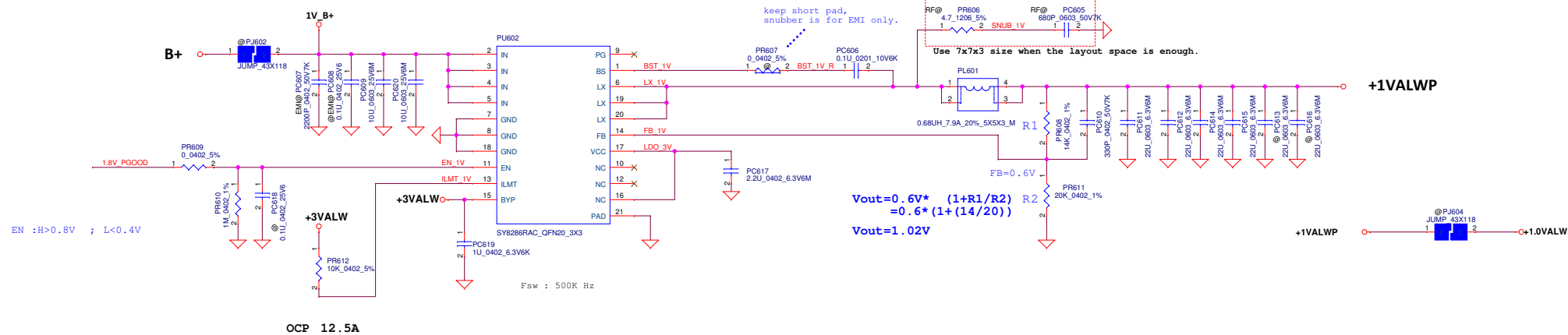
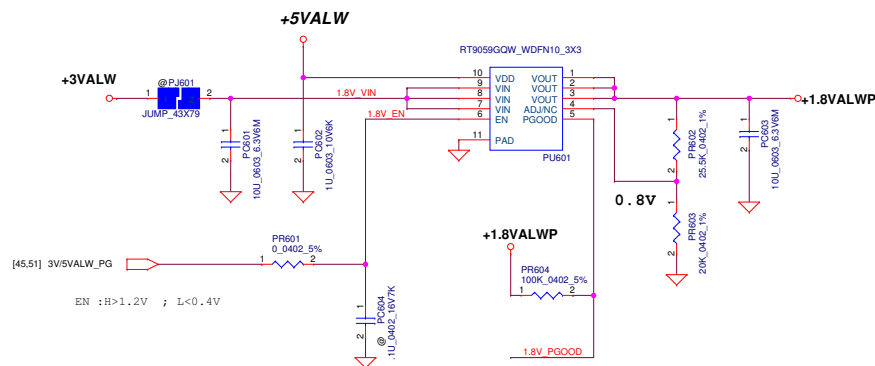
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Date:						Tuesday, December 19, 2017		Sheet 49 of 59			





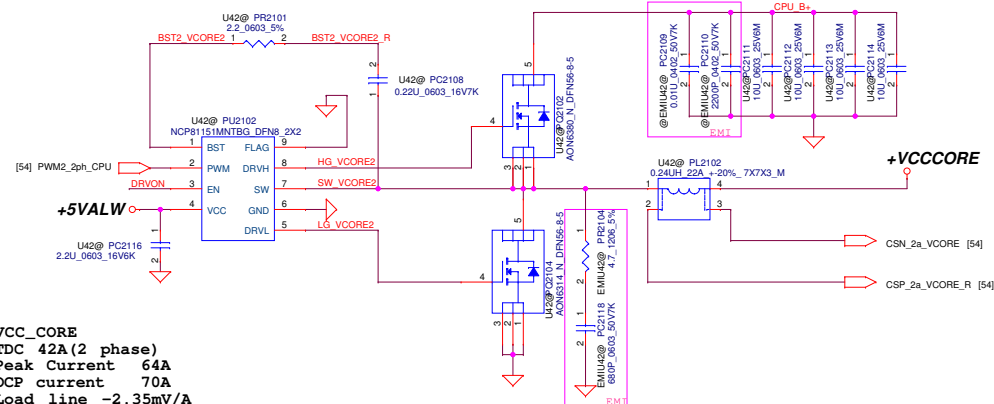
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Size	Document Number	VE	Sheet	Rev
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Date:	Tuesday, December 19, 2017	Sheet	51	of 59



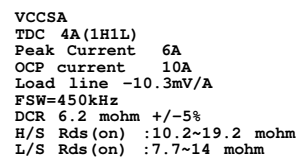
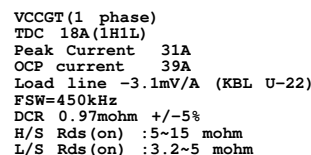


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VCC\_CORE  
TDC 42A(2 phase)  
Peak Current 64A  
OCP current 70A  
Load line -2.35mV/A  
FSW=450kHz  
DCR 0.97mohm +/-5%  
H/S Rds(on) :5~15 mohm  
L/S Rds(on) :3.2~5 mohm



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					VE
				Date:	Tuesday, December 19, 2017
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+VCCORE

+VCCORE

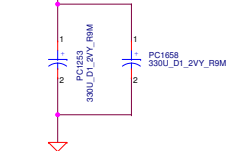
+VCCSA

VCCORE Place on CPU Back Side

U22  
22U\_0603 \* 10 (33) pcs  
1U\_0201 \* 35 (43) pcs  
330U\_D2 \* 2 pcs

U42  
22U\_0603 \* 10 (33) pcs  
1U\_0201 \* 35 (43) pcs  
330U\_D2 \* 2 pcs

+VCCORE



+VCCGT

+VCCGT

+VCCORE

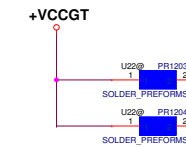
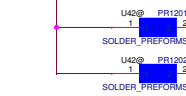
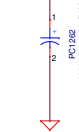
+VCC\_GT\_+VCC\_CORE

+VCCGT

VCCGT Place on CPU Back Side

22U\_0603 \* 28 (38) pcs  
1U\_0201 \* 12 (21) pcs  
330U\_D2 \* 1 pcs

+VCCGT



VCC\_CORE output cap(36.4), VCC\_GT output cap(36.5), VCC\_SA output cap(36.6), VCC\_IAGT out cap(36.7)

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Issued Date	2017/03/09	Deciphered Date
Deciphered Date	2018/06/30	2018/06/30
Title	PWR- CPU BACK SIDE MLCC	Rev
Document Number	VE	0.1
Date	Tuesday, December 19, 2017	Sheet 56 of 59

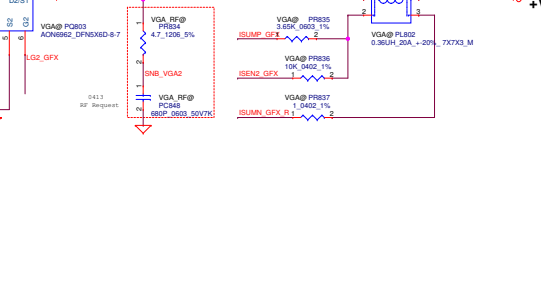
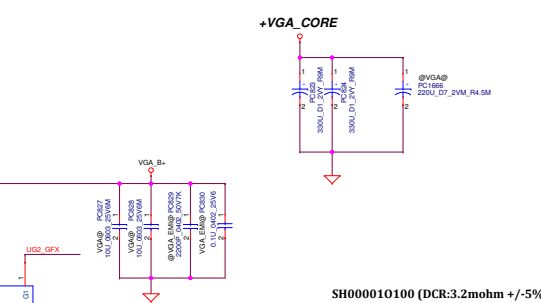
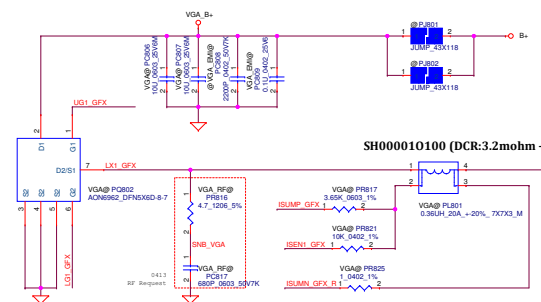
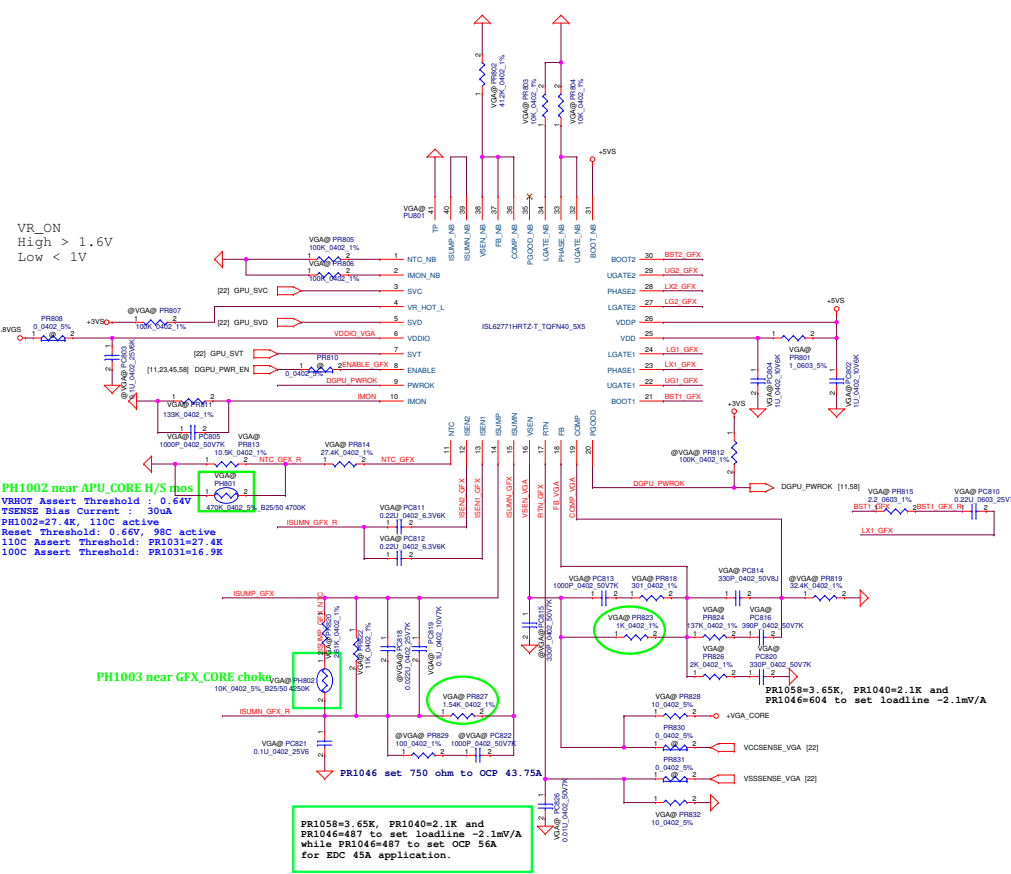
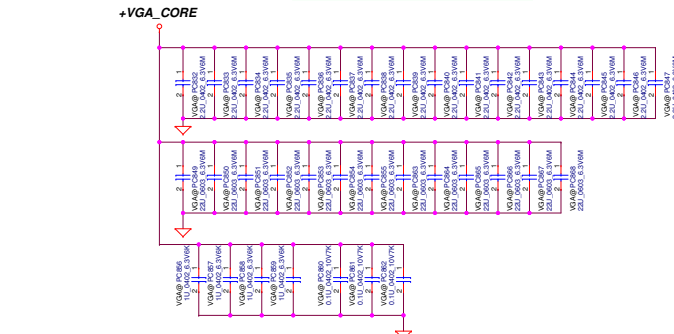


VR\_ON  
High > 1.6V  
Low < 1V

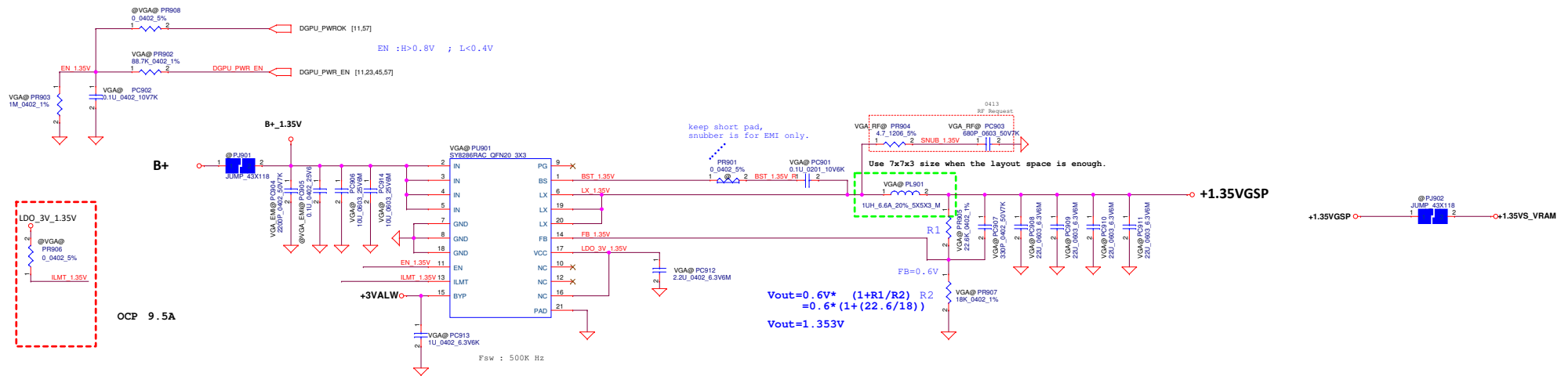
PH1002 near APU\_CORE H/S mos  
VRHOT Assert Threshold : 0.64V  
TSENSE Bias Current : 30uA  
PR1002=27.4K, 110C active  
Reset Threshold: 0.66V, 98C active  
110C Assert Threshold: PR1031=27.4K  
100C Assert Threshold: PR1031=16.9K

PH1003 near GFX\_CORE chokid  
VGA@ PR802  
10K, 0.0402, 5%, 0.25/50 4700K

PR1058=3.65K, PR1040=2.1K and  
PR1046=604 to set loadline ~2.1mV/A  
for EDC 45A application.



GFX\_core  
TDC 30 (1H1L)  
Peak Current 45A  
OCF current > 56A  
Load line ~2.1mV/A  
FSW=400kHz  
DCR 0.98mohm +/-5%  
TYP  
H/S Rds(on) :11.7mohm , 14mohm  
L/S Rds(on) :2.7mohm , 3.3mohm



Item	Reason for change	PG#	Modify List	Date	Phase
1					

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2017/11/15	Deciphered Date	2018/12/31	Title
					PIR (PWR)
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		C	LA-E981P	0.1	
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